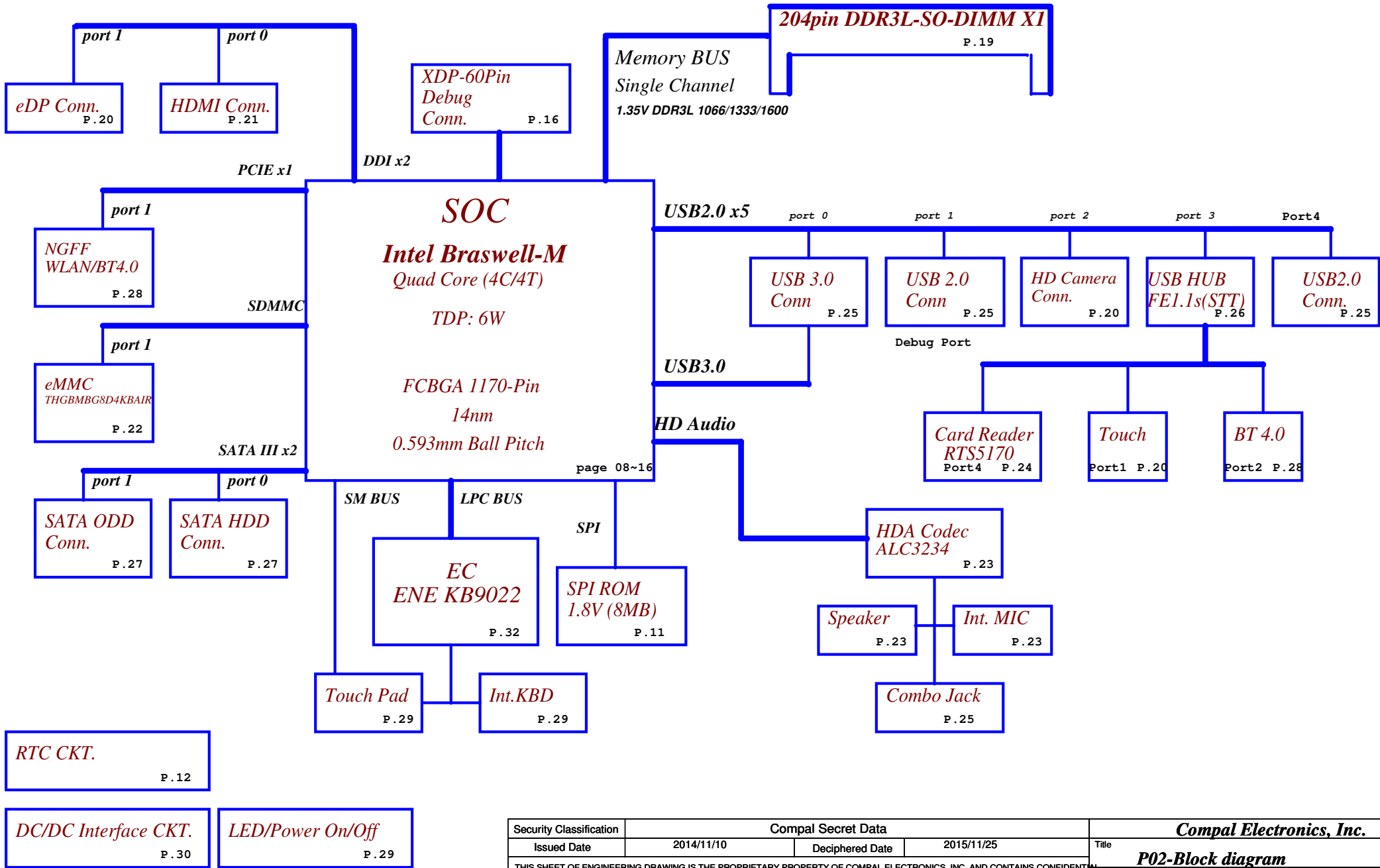


Compal Confidential
Schematic Document
Intel Braswell M
UMA

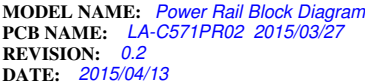
2015-6-09 Rev: 1.0

ZZZ PCB®
PCB 1EE LA-C571P REV1 M/B 2
DA6001DX010

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			Doc#	Rev
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Voltage Rails

Power Plane	Description	S0	S3	S4/S5
VIN	19V Adapter power supply	ON	ON	ON
BATT+	12V Battery power supply	ON	ON	ON
B+	AC or battery power rail for power circuit. (19V/12V)	ON	ON	ON
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.05VALW	+1.05v Always power rail	ON	ON	ON
+1.24VALW	+1.24v Always power rail	ON	ON	ON
+1.8VALW	+1.8v Always power rail	ON	ON	ON
+3VALW	+3.3v Always power rail	ON	ON	ON
+3V_SOC	+3V_SOC Always power rail	ON	ON	ON
+5VALW	+5.0v Always power rail	ON	ON	ON
+1.35V	+1.35V power rail for DDR3L	ON	ON	OFF
+VCC_CORE	Core voltage for SOC	ON	OFF	OFF
+VGG_CORE	GFX voltage for SOC	ON	OFF	OFF
+0.675VS	+0.675V power rail for DDR3L Terminator	ON	OFF	OFF
+1.15VALW	+1.15VALW system power rail	ON	OFF	OFF
+1.35VS	+1.35v system power rail	ON	OFF	OFF
+1.5VS	+1.5v system power rail	ON	OFF	OFF
+1.8VS	+1.8v system power rail	ON	OFF	OFF
+3VS	+3.3v system power rail	ON	OFF	OFF
+5VS	+5.0v system power rail	ON	OFF	OFF
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

Board ID / SKU ID Table for AD channel

Board ID Table for AD channel					
Vcc	3.3V +/- 1%				
Ra	100K +/- 1%				
Board ID	Rb	VAD_BID_min	VAD_BID_typ	VAD_BID_max	EC_AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.551V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xEE
19	NC	3.000V	3.300V	3.300V	0xEF - 0xFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0

BOM Option Table

Item	BOM Structure
Unpop	@
Connector	CONN@
XDP (Debug Port)	XDP@
EMC requirement	EMI@
EMC requirement unpop	NEMI@
LPC18	LPC18@
LPC33	LPC33@
Rvs. RF requirement	RF@
ESD requirement	ESD@
XDP (Debug Port) unpop	NXDP@
ESD requirement unpop	NESD@
For JUMP	JP@
For PCB	PCB@
For CPU	SOC@ SOC1@
SATA re-Driver	601@
Test Point	TP@
SATA re-Driver unpop	N601@

43 level BOM table

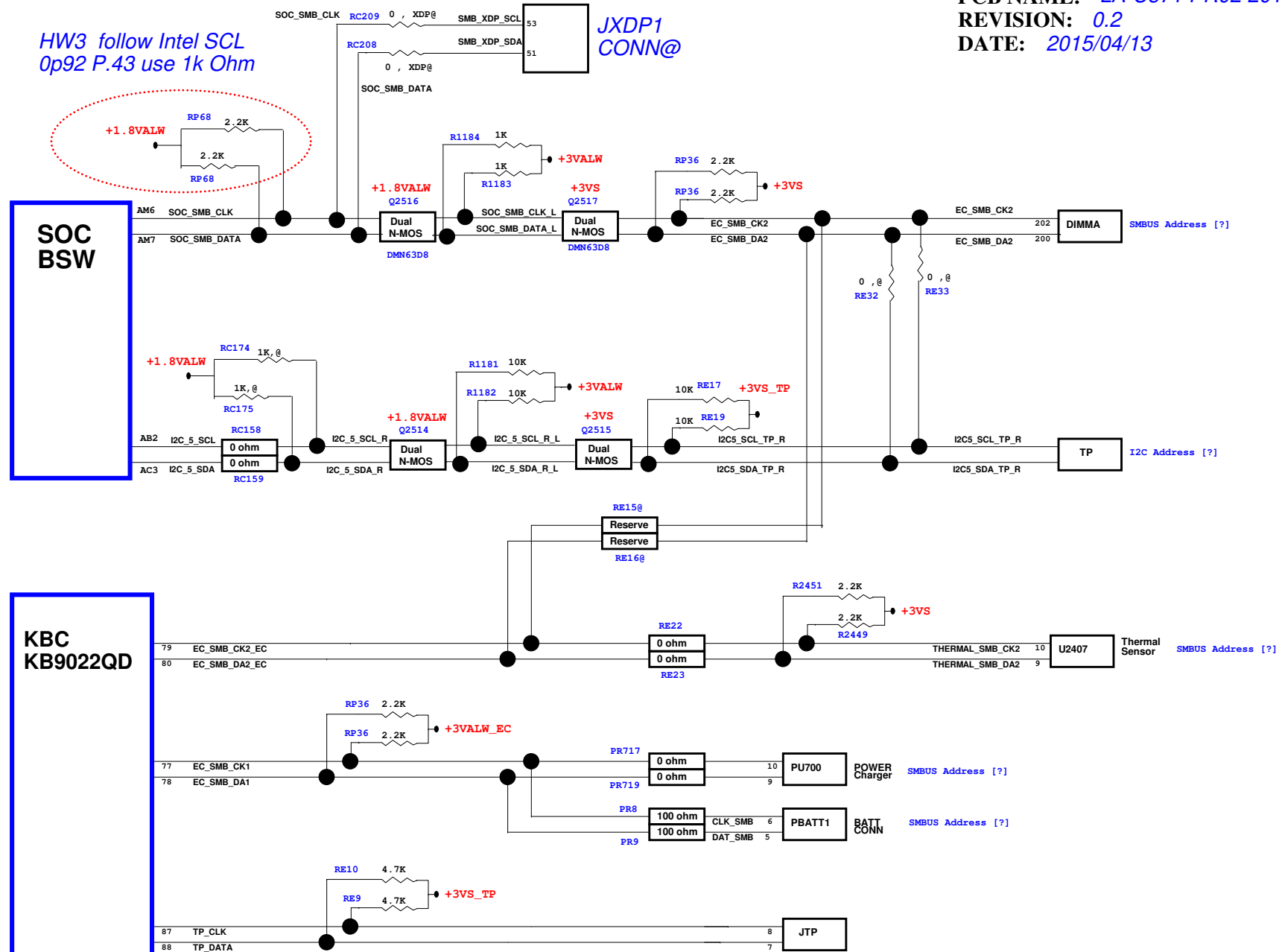
43 Level	Description	BOM Structure
4319Y031L01	MB AC571 AAL14 BSW U PEN HDMI	EMI@/ESD@/XDP@/LPC33@/PCB@/ODD@/SOC@/601@/N601@/PARADE@
4319Y031L02	MB AC571 AAL14 BSW U CEL HDMI	EMI@/ESD@/XDP@/LPC33@/PCB@/ODD@/SOC1@/601@/N601@/PARADE@

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MODEL NAME: *SMBus Block Diagram*
PCB NAME: *LA-C571 PR02 2015/03/27*
REVISION: *0.2*
DATE: *2015/04/13*

*HW3 follow Intel SCL
Op92 P.43 use 1k Ohm*

*JXDP1
CONN@*

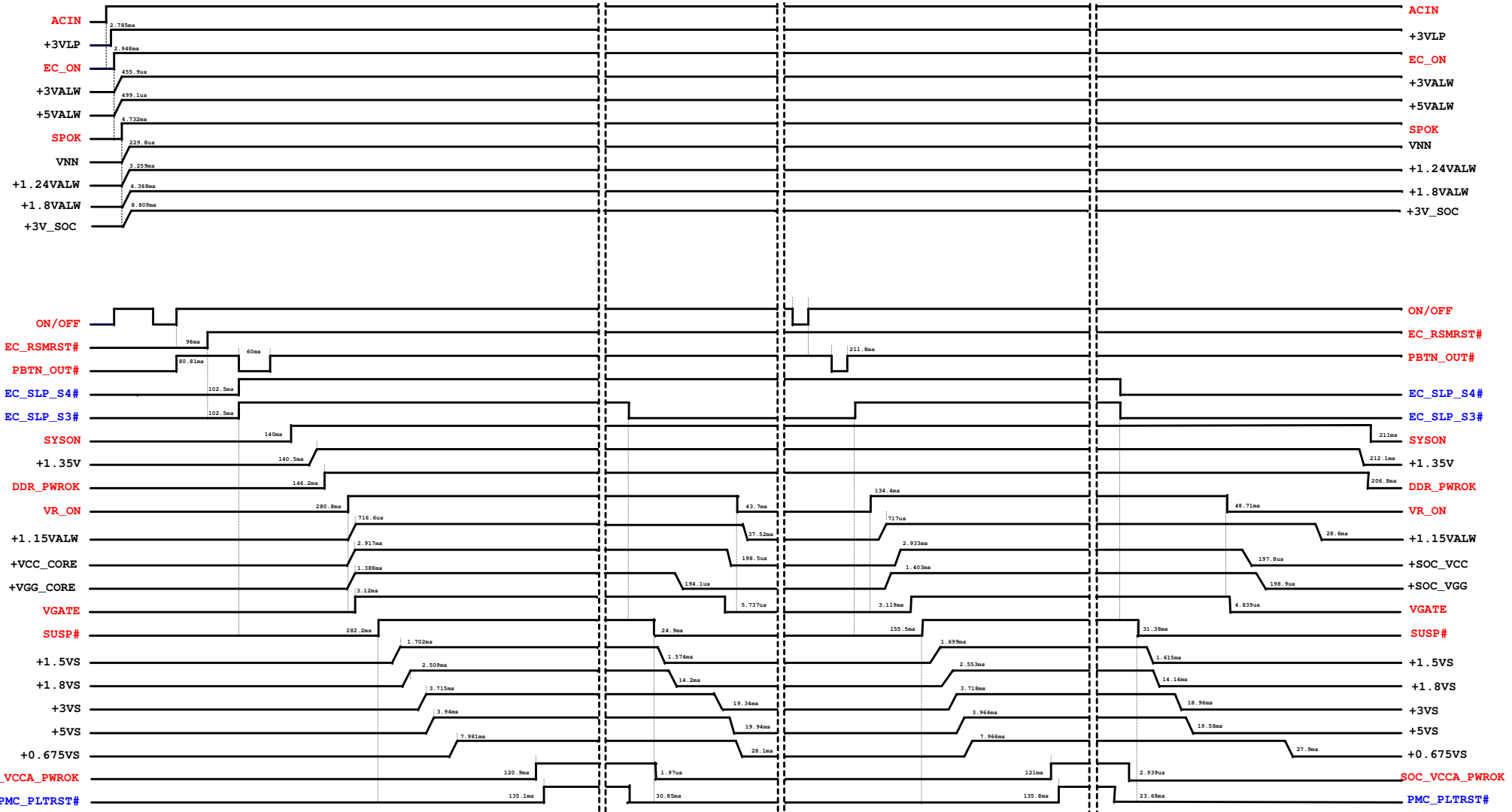


S5->S0

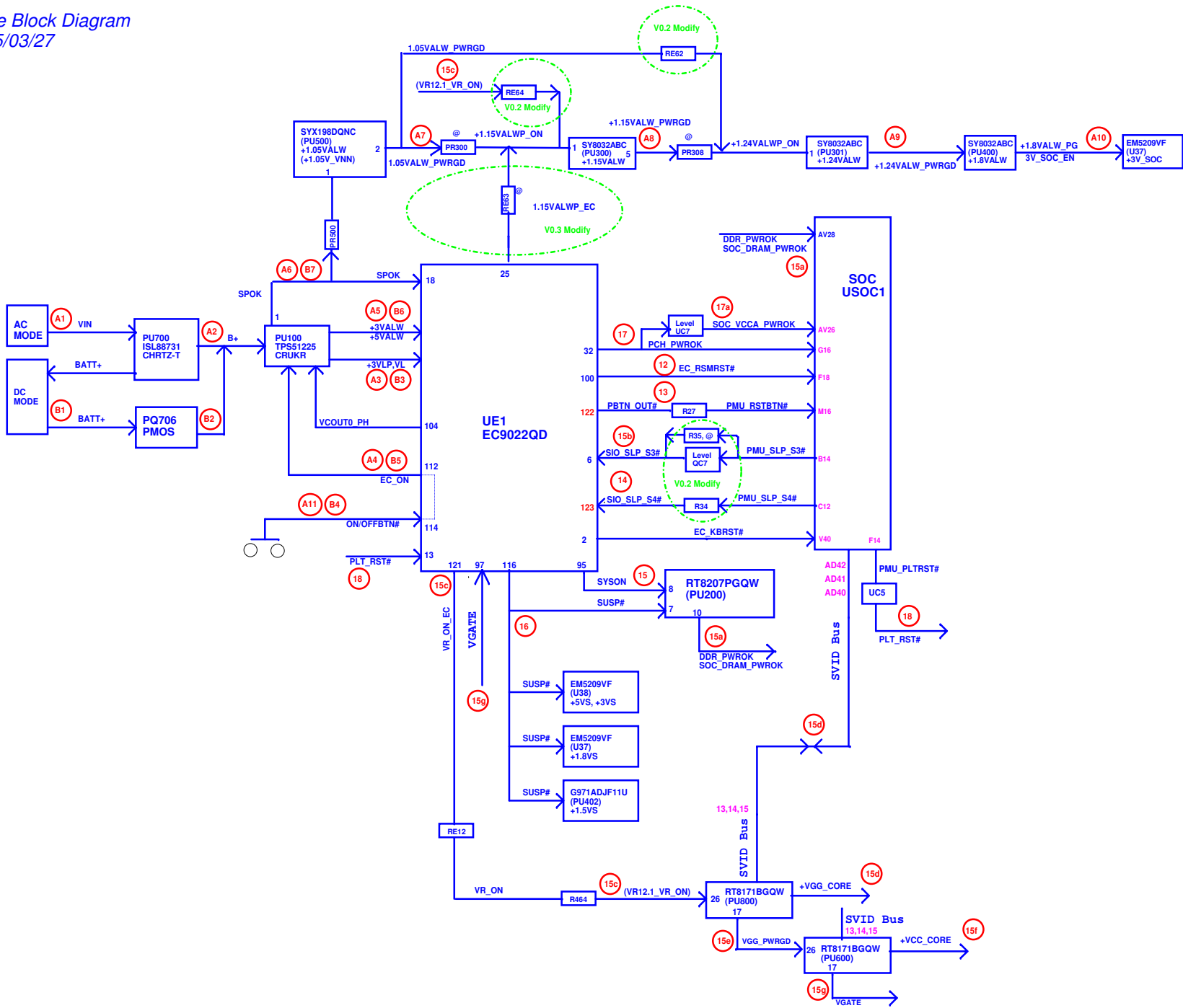
S0->S3

S3->S0

S0->S5



MODEL NAME: Power Sequence Block Diagram
PCB NAME: LA-C571PR02 2015/03/27
REVISION: 0.2
DATE: 2015/04/13



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Main Func = CPU

UC1
SOC@

S IC A31 FH806501715806 QJMS C0 1.6G
Part Number = SA00008U52L

UC1
SOC@

S IC A31 FH806501715814 QJ4V C0 1.6G
Part Number = SA00008U52L

<19> DDR_M0_DQS[0..7]
<19> DDR_M0_DQS#0..7]

Place close to SOC pins

+1.35V
@
RC5
10K_0402_1%
Pull high 10K on page 36

SOC_DRAM_PWROK RC180 1

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UC1A

CHV_MCP_EDS

DDR3

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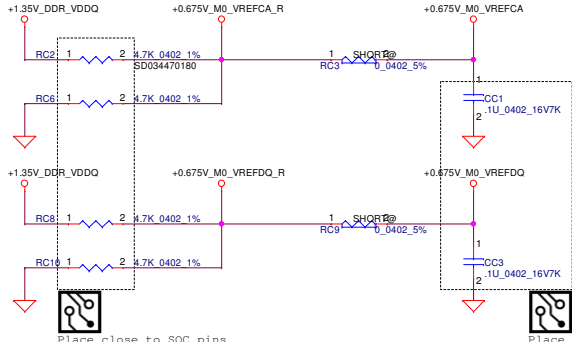
DDR3

DDR3

DDR3

Power Name and Connection Check OK

8 mils minimum for maximum of 300 mils in breakout area

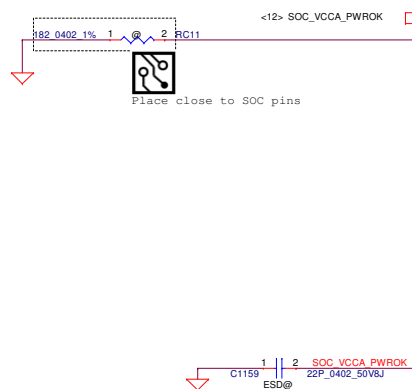


Place close to SOC pins

Place close to SOC pins

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Main Func = CPU



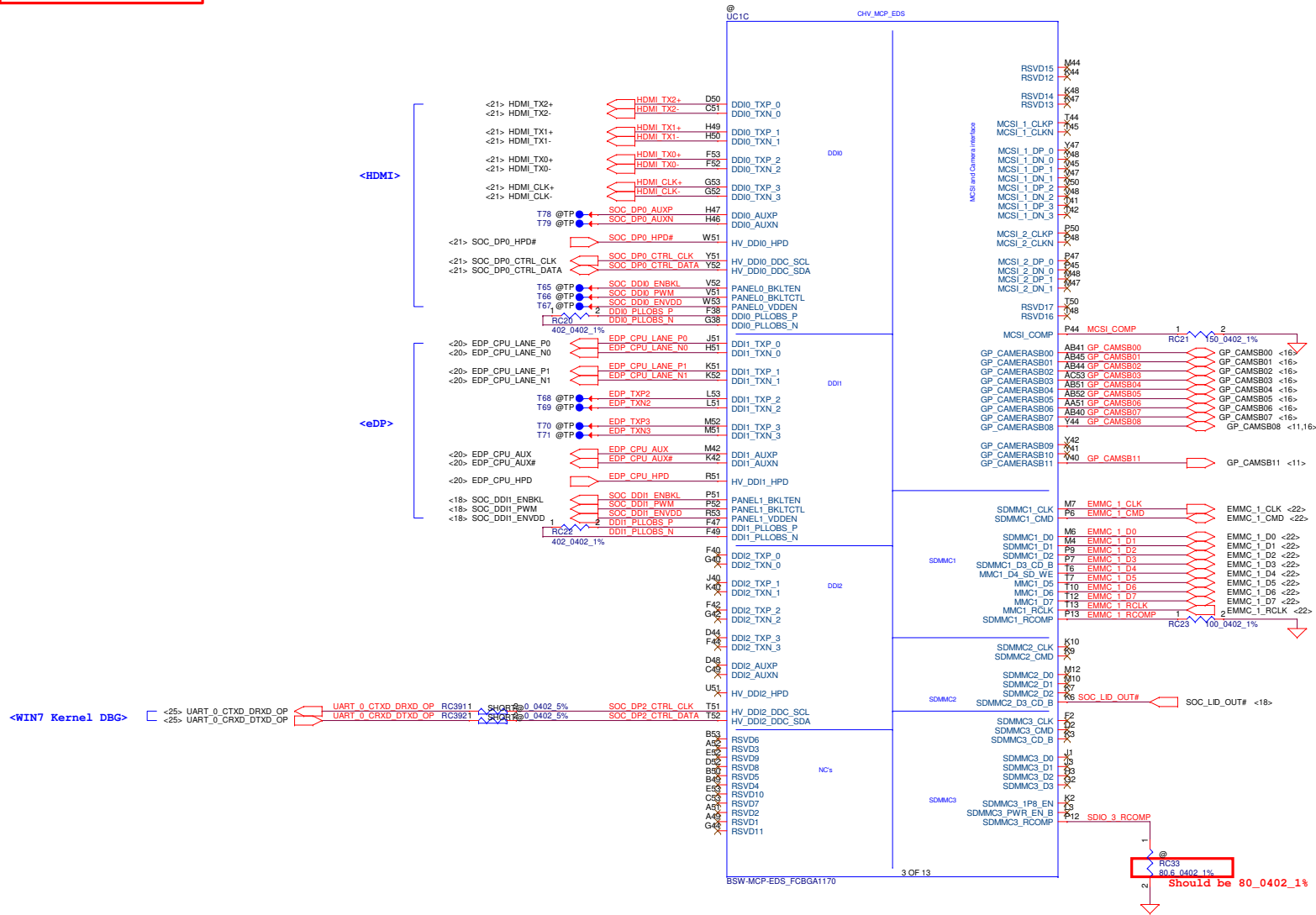
@ UC1B CHY_MCP_EDS		
DDR1		
BD5	DDR3_M1_MA_15	BG21
BD6	DDR3_M1_MA_14	BH26
BF16	DDR3_M1_MA_13	BJ25
BB5	DDR3_M1_MA_12	BG26
BJ6	DDR3_M1_MA_11	BG22
BE2	DDR3_M1_MA_10	BH20
BD10	DDR3_M1_MA_9	BG25
BE8	DDR3_M1_MA_8	BH21
BB8	DDR3_M1_MA_7	BD26
BH6	DDR3_M1_MA_6	BF24
BD12	DDR3_M1_MA_5	BA20
BH12	DDR3_M1_MA_4	BD20
BJ6	DDR3_M1_MA_3	BD24
BC12	DDR3_M1_MA_2	BA22
BE1	DDR3_M1_MA_1	BD20
BF2	DDR3_M1_MA_0	BF20
AY18	DDR3_M1_BS_2	AV22
BH1	DDR3_M1_BS_1	AV20
BC9	DDR3_M1_BS_0	BD18
BA18	DDR3_M1_CASB	BF18
BH10	DDR3_M1_RASB	AU22
AU18	DDR3_M1_WEB	AU20
AY18	DDR3_M1_CSB_1	BA18
AY18	DDR3_M1_CSB_0	BC18
BD16	DDR3_M1_CK_1	BH16
BF16	DDR3_M1_CKB_1	BH18
AY12	DDR3_M1_CKB_0	BJ13
BD14	DDR3_M1_CKE_1	BH12
BF18	DDR3_M1_CK_0	BJ17
BB10	DDR3_M1_CKB_0	BG17
AT24	DDR3_M1_CKE_0	BG11
AU24	RSVD1	BD12
AV18	RSVD2	BB3
BA18	DDR3_M1_DQ_31	BW11
AY18	DDR3_M1_DQ_30	BC2
AT26	DDR3_M1_DQ_29	BW3
AU26	DDR3_M1_DQ_28	AV3
BA12	DDR3_M1_OCAVREF	BC1
AY26	DDR3_M1_ODQVREF	AV2
BA26	DDR3_M1_DRAMRSTB	BD2
BA26	DDR3_VCCA_PWROK	AV12
BA26	DDR3_M1_RCOMP	AP13
BH24	DDR3_M1_DM_7	AV13
BD22	DDR3_M1_DM_6	AT10
AY18	DDR3_M1_DM_5	AP14
BG18	DDR3_M1_DM_4	AT16
BA18	DDR3_M1_DM_3	AP12
AP18	DDR3_M1_DM_2	AT14
AP2	DDR3_M1_DM_1	AV9
BH22	DDR3_M1_DM_0	AV4
BG26	DDR3_M1_DQS_7	AT14
BC26	DDR3_M1_DQS_6	AP7
AT26	DDR3_M1_DQS_5	AV4
BH18	DDR3_M1_DQS_4	AV6
BG18	DDR3_M1_DQS_3	AT7
BA18	DDR3_M1_DQS_2	AP6
AT18	DDR3_M1_DQS_1	AP3
AV18	DDR3_M1_DQS_0	BR1
AM18	DDR3_M1_DQS_0	AK2
AM18	DDR3_M1_DQS_0	BL1
AM18	DDR3_M1_DQS_0	BR3
AM18	DDR3_M1_DQS_0	AT2
AM18	DDR3_M1_DQS_0	BL3
AM18	DDR3_M1_DQS_0	AK3
AM18	DDR3_M1_DQS_0	AK3

2 OF 13

BSW-MCP-EDS_FCBGA1170

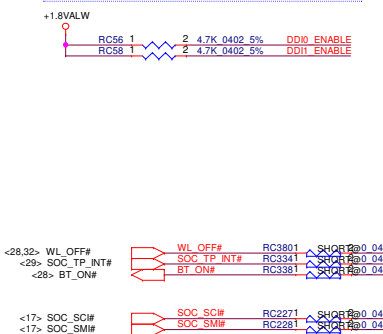
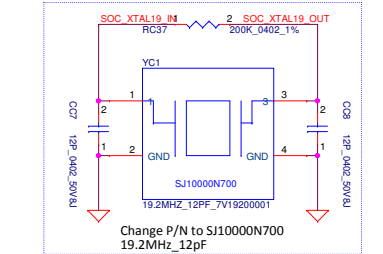
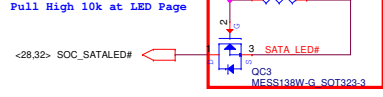
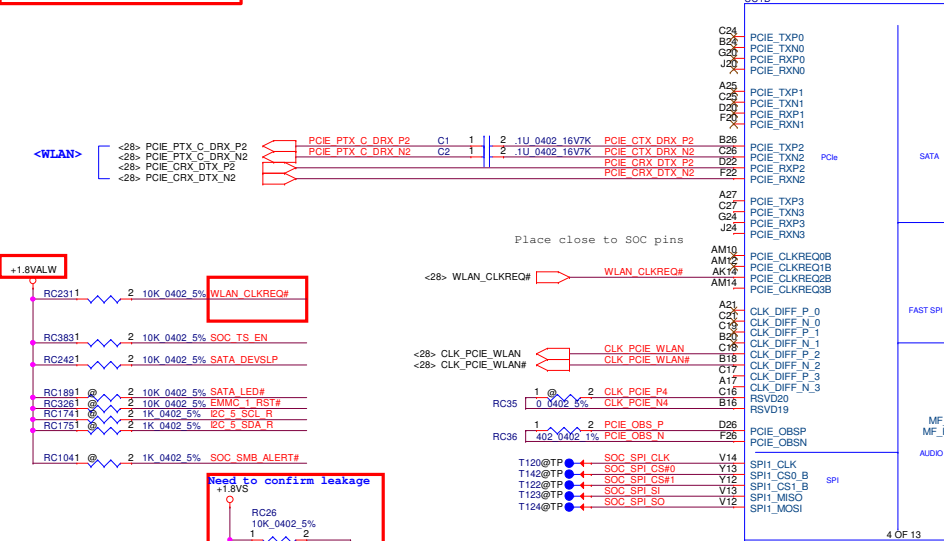
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				Tuesday, June 16, 2015	1.0
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Main Func = CPU



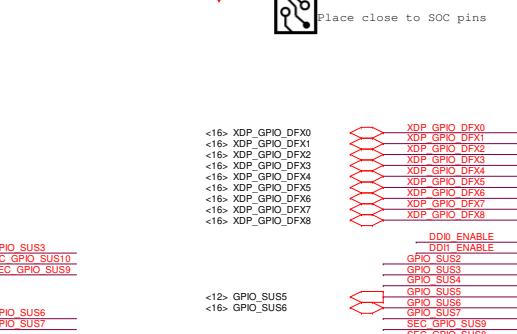
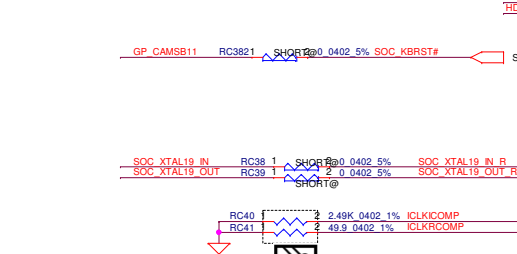
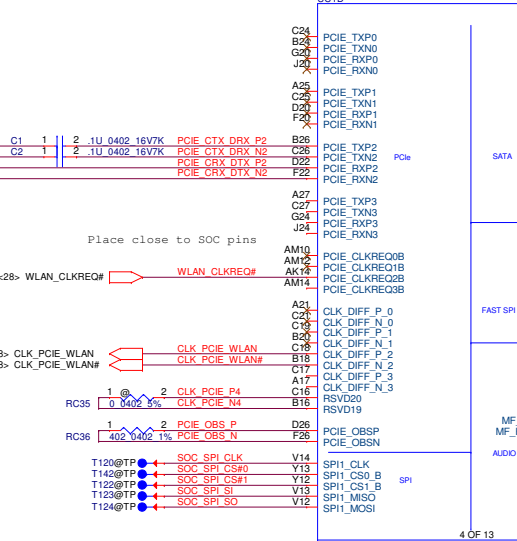
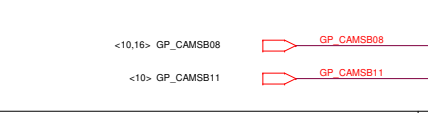
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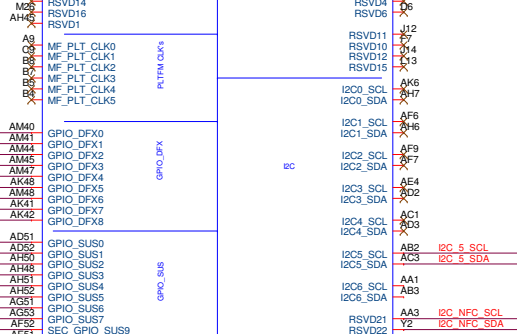
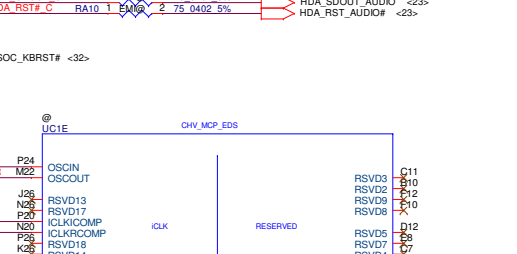
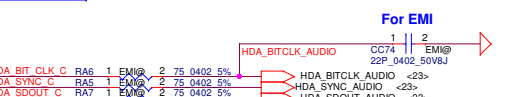
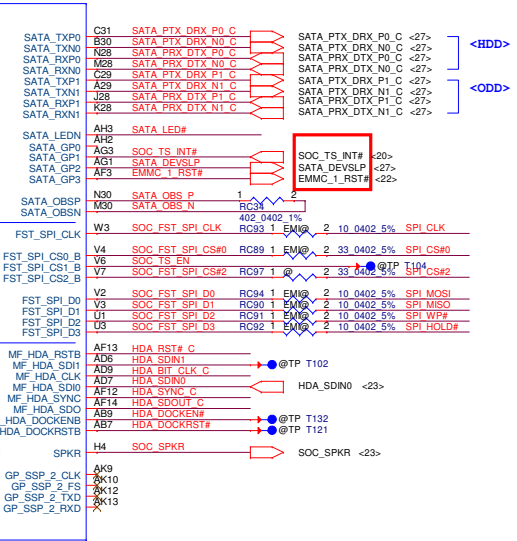
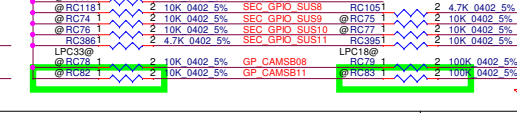
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EC_SMI# PH +3VALW_EC Page 32 不上件



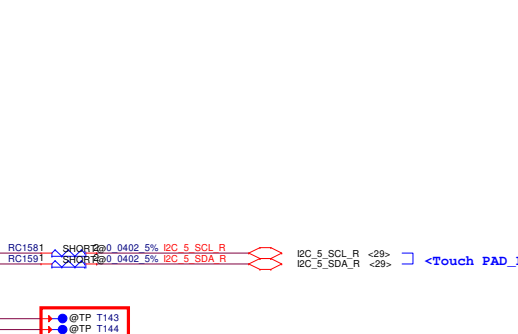
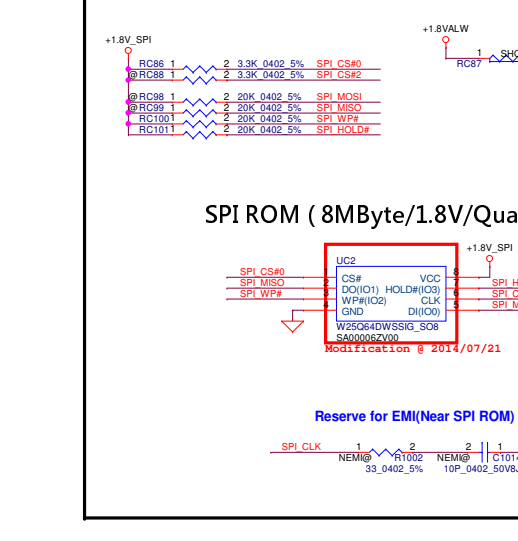
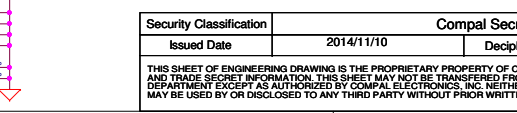
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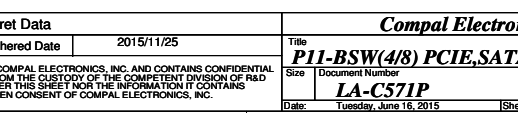
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SOC_SMI# PH +1.8VALW Page 17 不上件
EC_SMI# PH +3VALW_EC Page 32 不上件

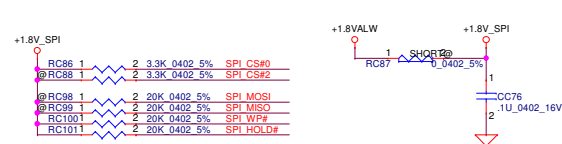


GPIO_SUS6 H +1.8VALW Page 11 不上件
SOC_SCI# PH +1.8VS Page 17 for 9022 上件
EC_SCI# PH +3.3VS Page 32 for 9012 不上件

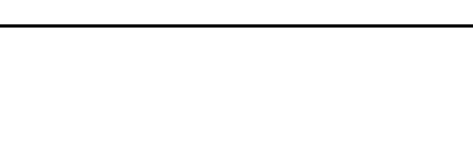
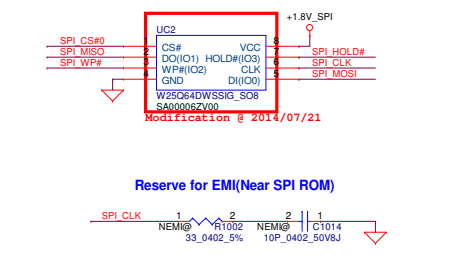
GPIO_SUS7 H +1.8VALW Page 11 不上件
SOC_SMI# PH +1.8VALW Page 17 不上件
EC_SMI# PH +3VALW_EC Page 32 不上件



BIOS ROM

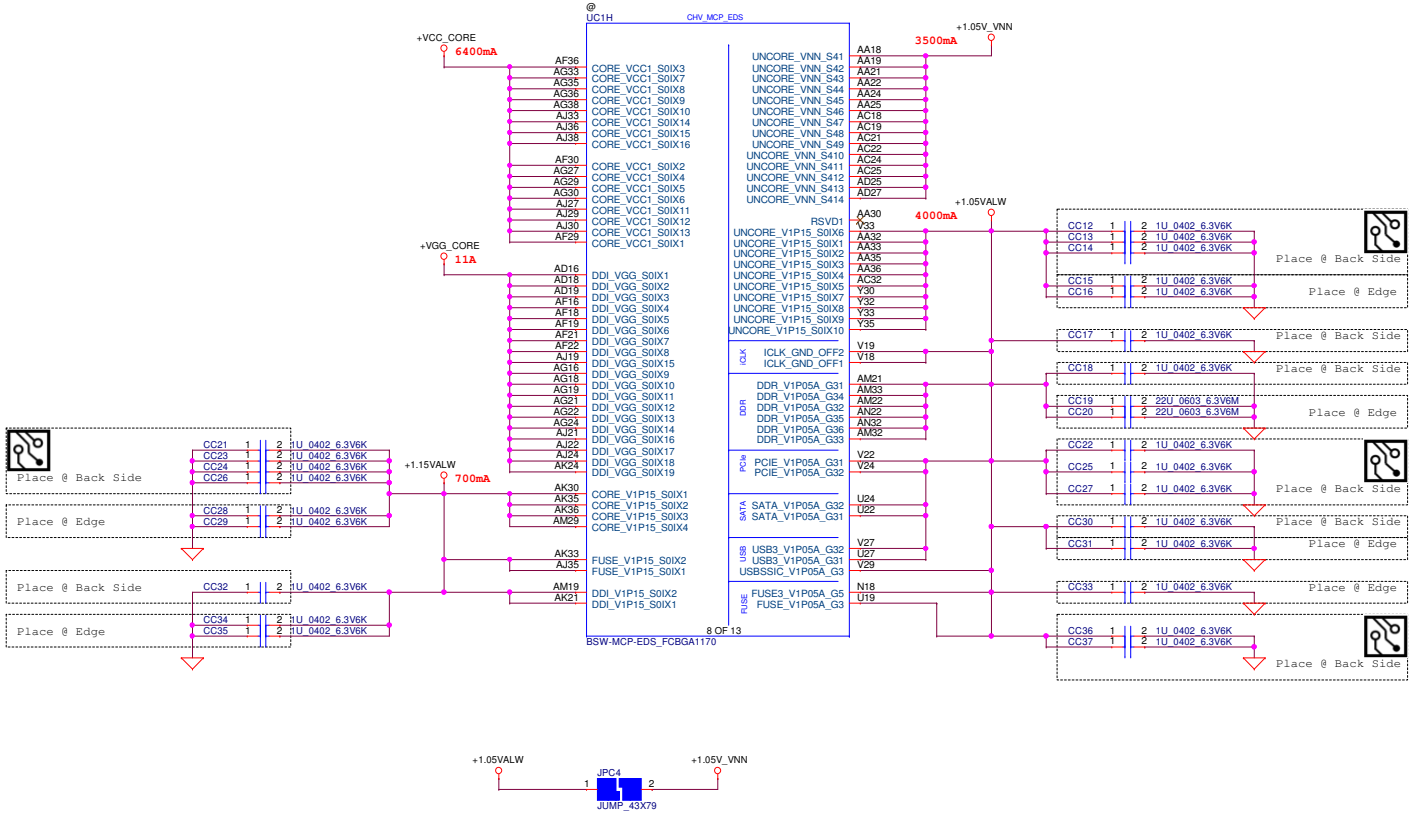


SPI ROM (8MByte/1.8V/Quad-IO)



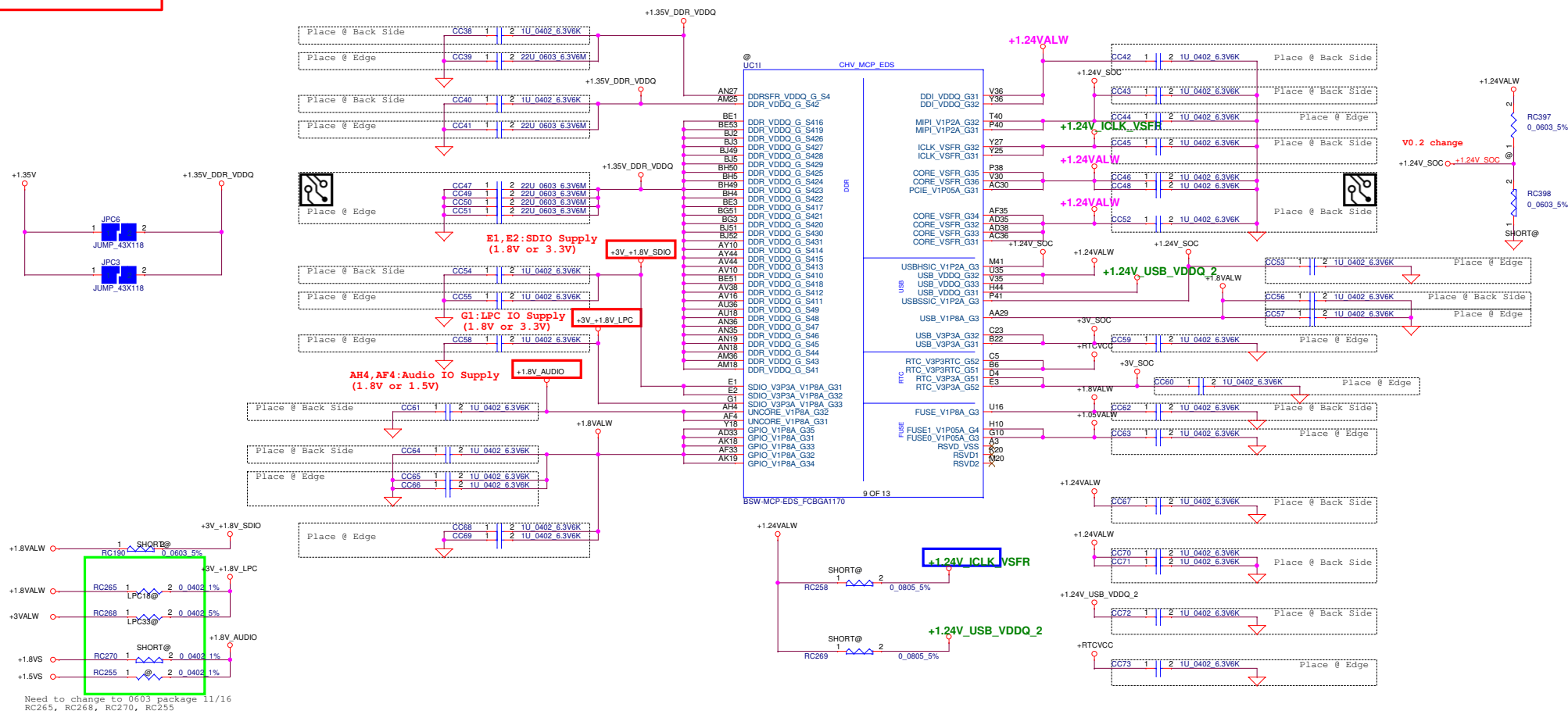
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/11/10	Deciphered Date	2015/11/25	Title	P11-BSW(4/8) PCIE,SATA,I2C,CLK
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					LA-C571P
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Main Func = CPU



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Issued Date	2014/11/10	Deciphered Date	2015/11/25	Title	P13-BSW(6/8) PWR1	
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					LA-C571P	1.0
				Date	Tuesday, June 16, 2015	Sheet 13 of 44

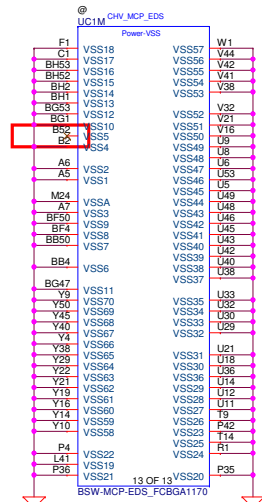
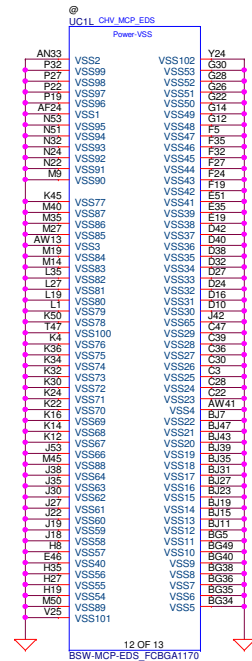
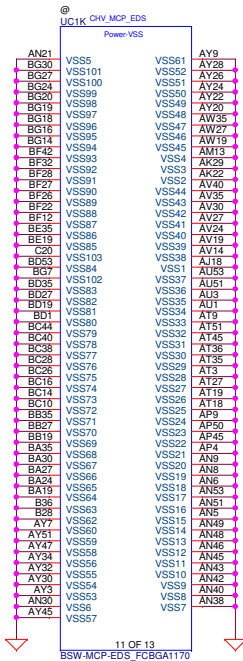
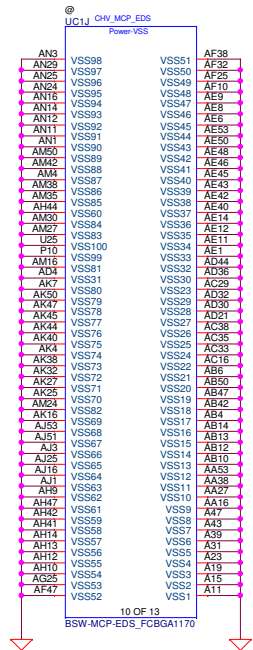
Main Func = CPU



NOTE:
+1.24V_MIP1, +1.24V_USBHSIC, +1.24V_USBSIC are +1.24V Only.
[PDG Rev0p92 P.55]
When SSIC, HSIC & CSI interface is not used, the following pins can be connected to ground:
CSI (T40, P40), USB HSIC (M41), USB SSIC (P41).

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					LA-C571P	1.0
				Date:	Tuesday, June 16, 2015	Sheet 14 of 44

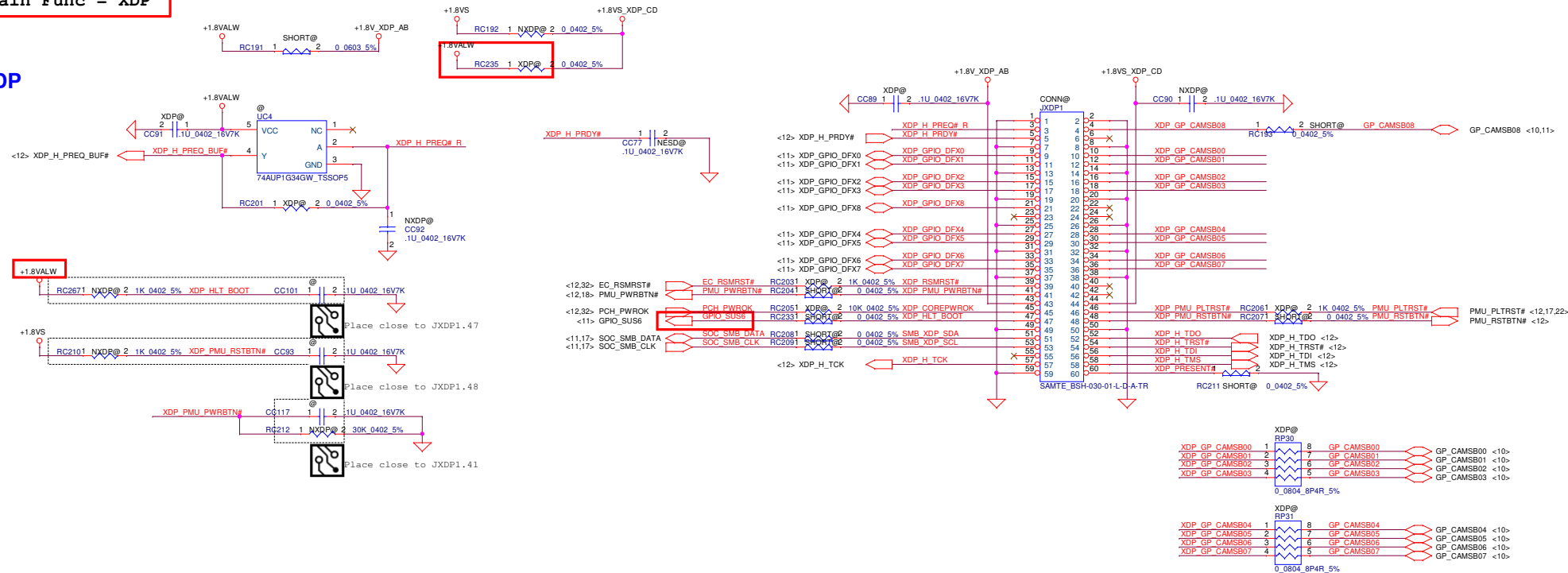
Main Func = CPU



Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2014/11/10	Deciphered Date	2015/11/25	Title	P15-BSW(8/8) GND	
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					LA-C571P	1.0
Date: Tuesday, June 16, 2015				Sheet	15	of 44


```
Main Func = XDP
```

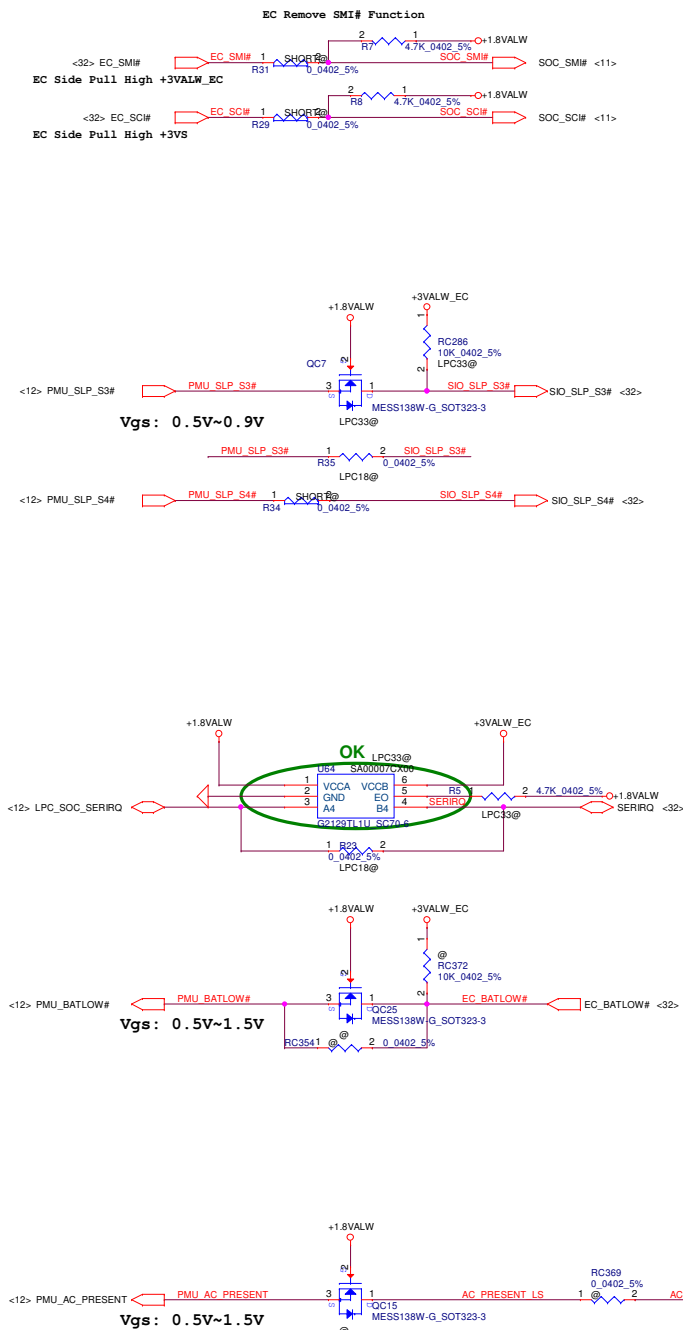
XDP



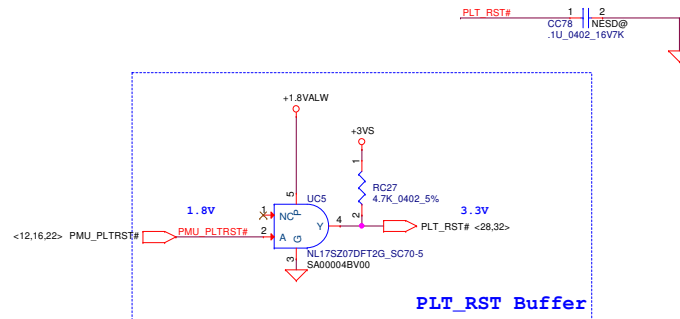
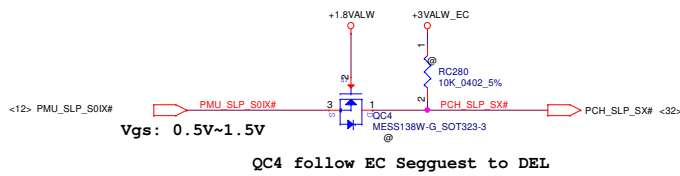
Security Classification		Compal Secret Data		Compal Electronics, Inc.					
Issued Date		2014/11/10	Deciphered Date		2015/11/25	Title			
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						Size	Document Number		Rev
						LA-C571P			1.0
Date:		Tuesday, June 16, 2015		Sheet	16	of 44			

Main Func = Level Shift

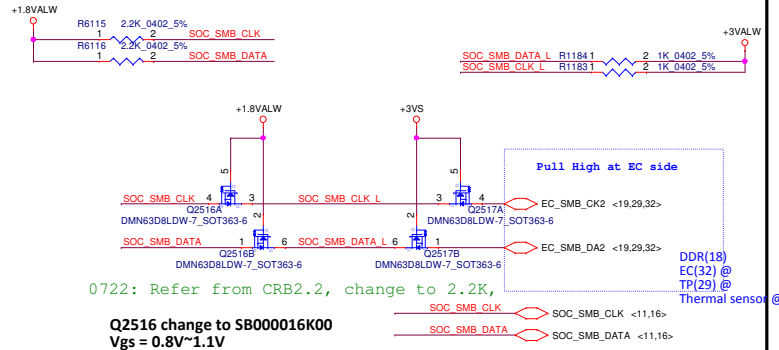
POWER ON SEQUENCE



POWER ON SEQUENCE



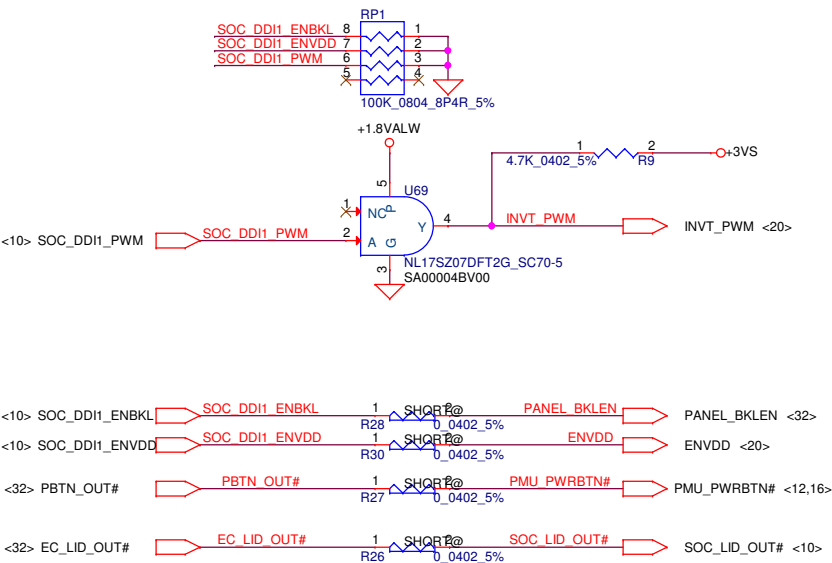
SMBUS
EC/Thermal Sensor/Touch Pad



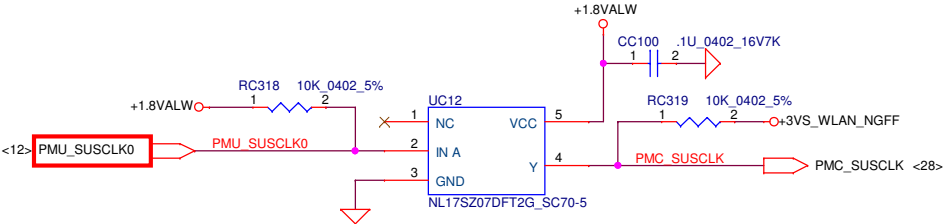
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/11/10	Deciphered Date	2015/11/25	Title	P17-Level Shift-1
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Main Func = Level Shift

eDP Control



WLAN



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Issued Date	2014/11/10	Deciphered Date	2015/11/25	Title	P18-Level Shift-2
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				Date:	Tuesday, June 16, 2015
				Sheet	18 of 44
				Rev	1.0

Main Func = DIMM

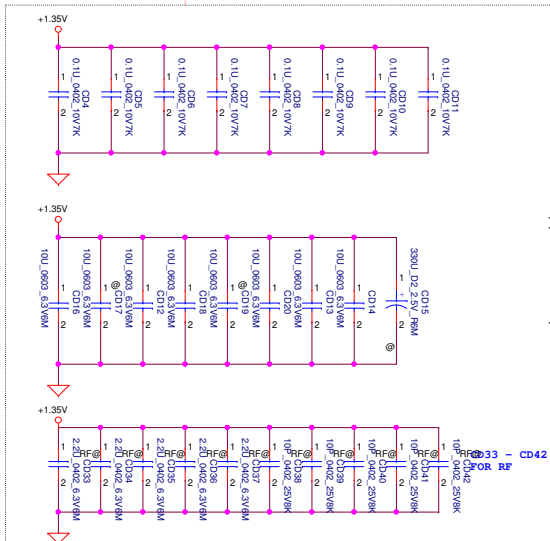
Populate RD1, De-Populate RD7 for Intel DDR3 VREFDQ multiple methods M1
Populate RD7, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

<8> DDR_M0_DM[4,7]
<8> DDR_M0_DM[0,3]
<8> DDR_M0_DQS[0,7]
<8> DDR_M0_DQS[0,7]
<8> DDR_M0_DQ[0,31]
<8> DDR_M0_DQ[0,31]
<8> DDR_M0_MA[0,15]

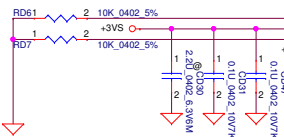
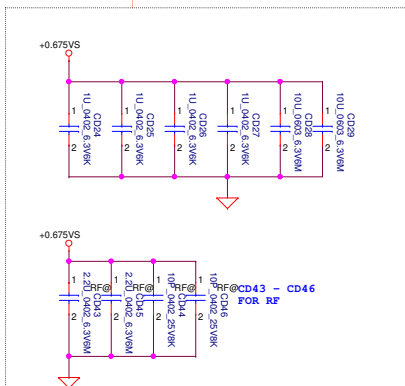
All VREF traces should have 10 mil trace width

Layout Note:
Place near JDIMM1

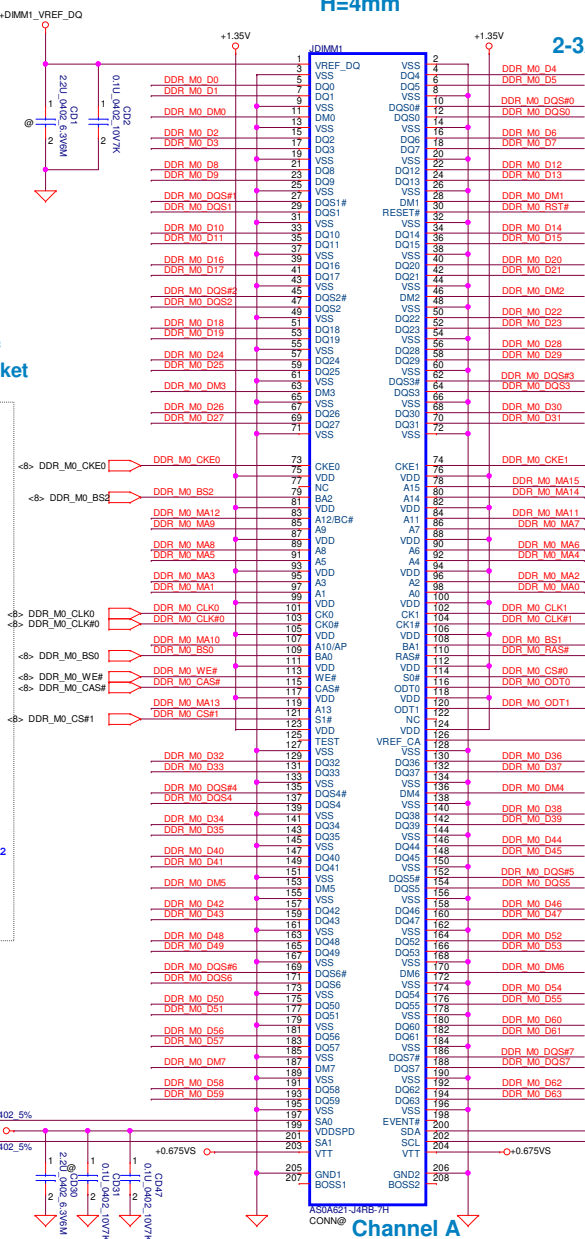
Note:
Check voltage tolerance of VREF_DQ at the DIMM socket



Layout Note:
Place near JDIMM1.203,204



ESD solution

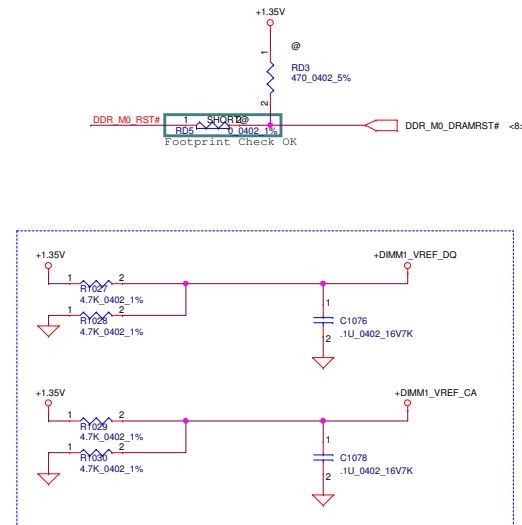


<Address: SA1:SA0=00 (A0H)>
DIMM_1 STD H:4mm

H=4mm

2-3A to 1 DIMMs/channel

CAD NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN

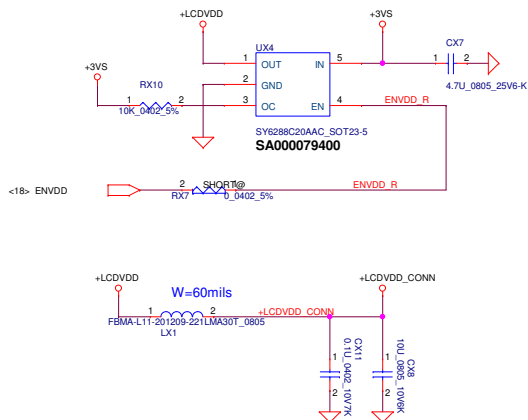


DDR_M0_ODT0 <8> DDR_M0_ODT0 <8>
DDR_M0_ODT1 <8> DDR_M0_ODT1 <8>
V0.2 change

Security Classification		Compal Secret Data		Title	
Issued Date	2014/11/10	Deciphered Date	2015/11/25	P19-DDRIII DIMMA	
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				LA-C57IP	
				Date: Tuesday, June 16, 2015	Sheet 19 of 44

Main Func = eDP

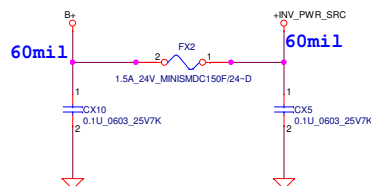
LCD PWR CTRL



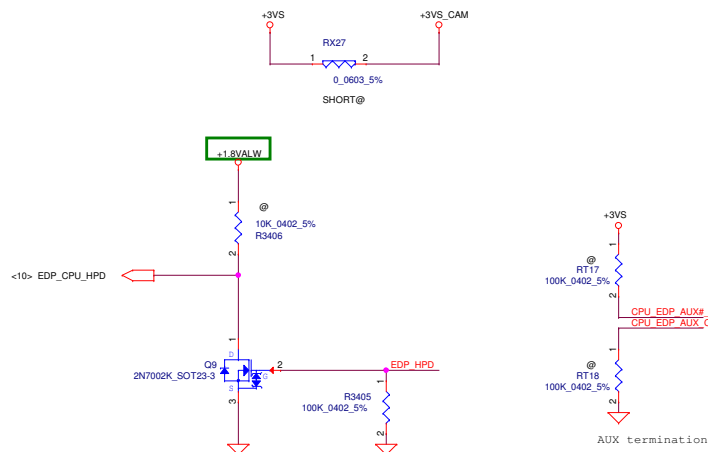
SS table

Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS

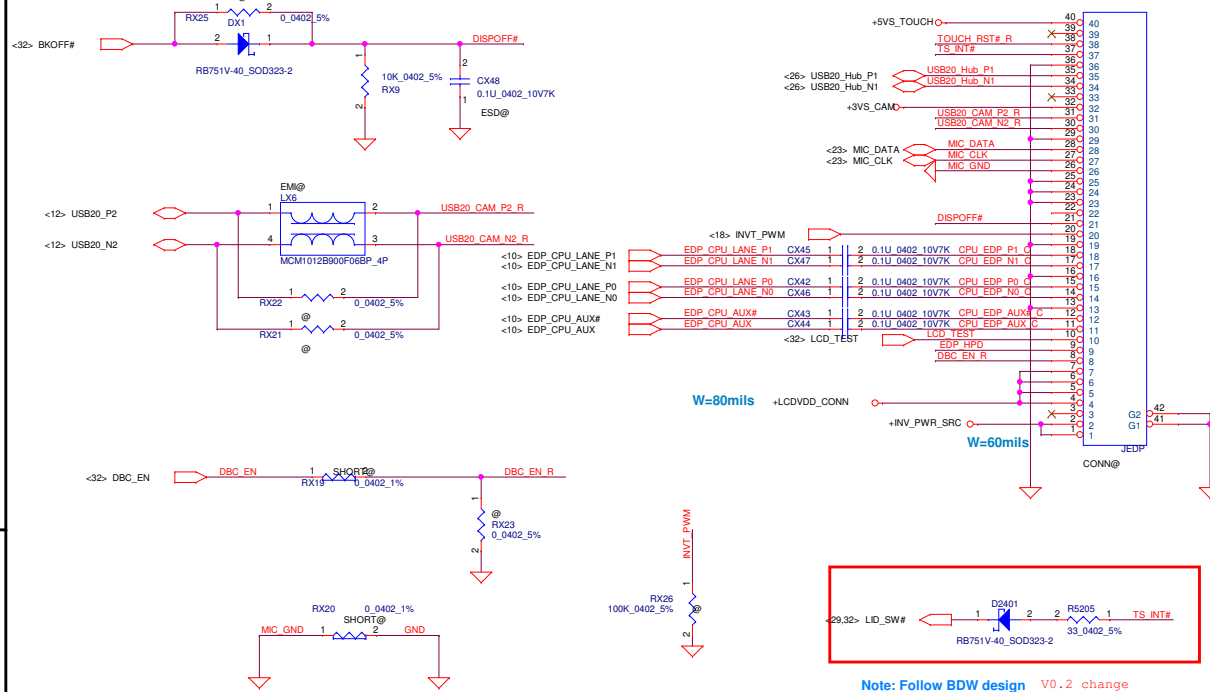
LCD backlight PWR CTRL



Webcam PWR CTRL

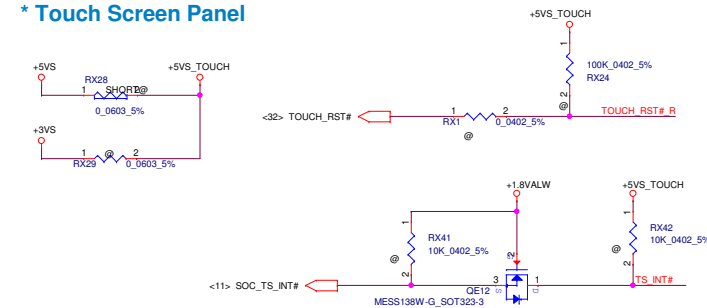


LCD Connector



Note: Follow BDW design V0.2 change

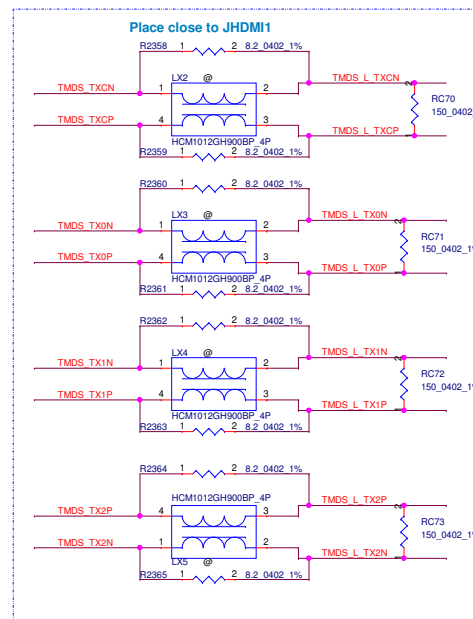
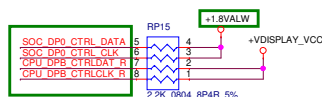
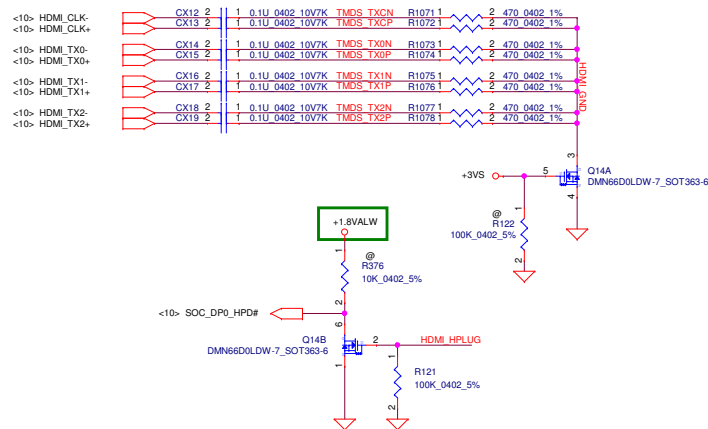
* Touch Screen Panel



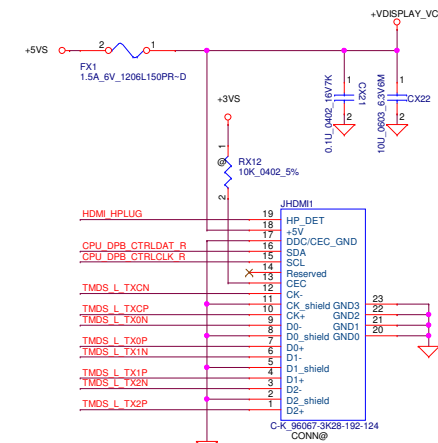
Closed to JEDP

Main Func = HDMI

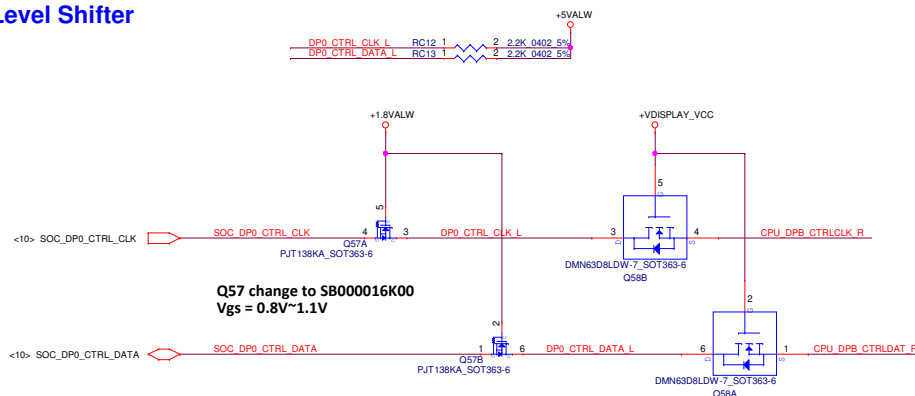
Part Number	Description
RO0000002HM	HDMI W/Logo:RO0000002HM



W=40mils



Level Shifter

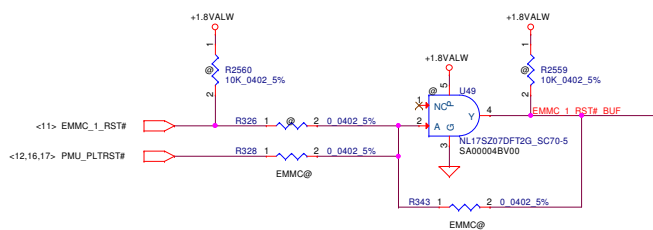
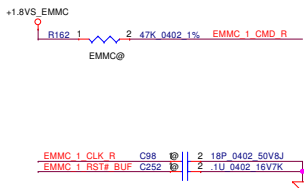
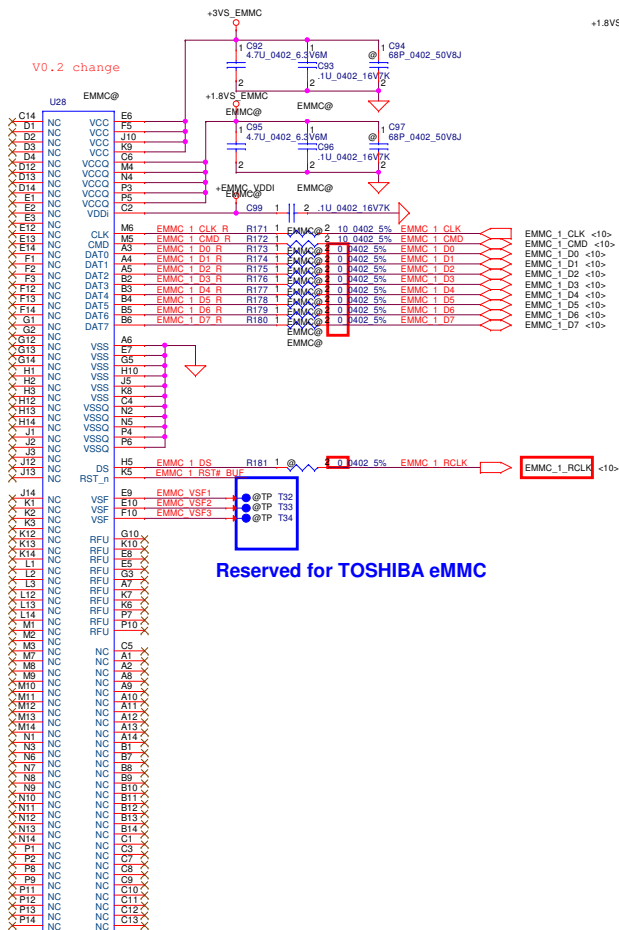
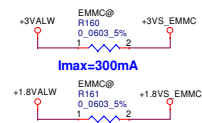


V0.2 change

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Security Classification		Compal Secret Data	
Issued Date		2014/11/10	
Deciphered Date		2015/11/25	
Title		P21-HDMI	
Document Number		LA-C571P	
Date		Tuesday, June 16, 2015	
Sheet		21 of 44	

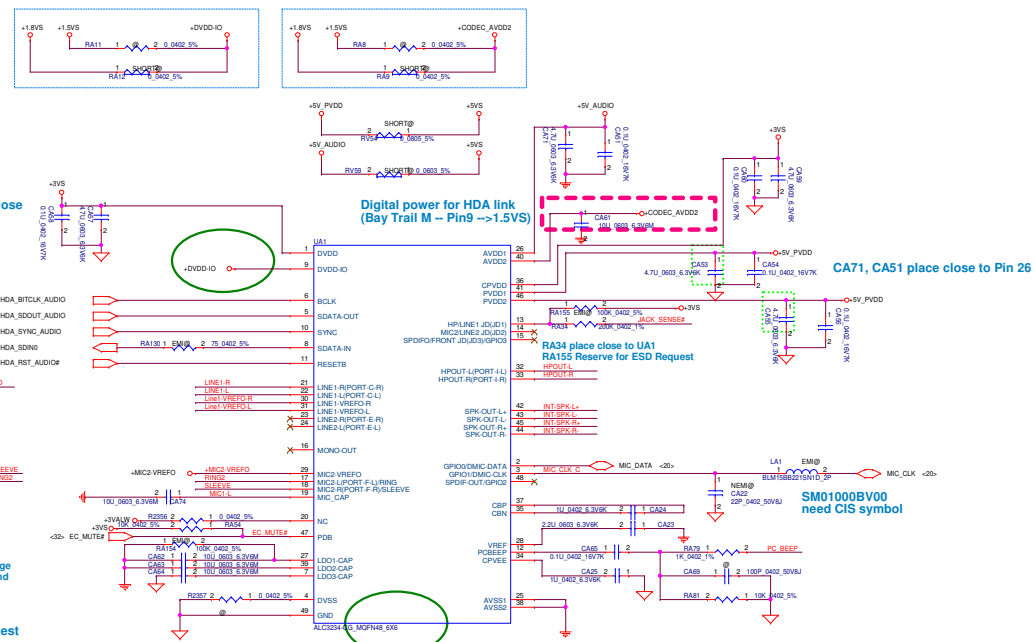
Main Func = eMMC

EMMC

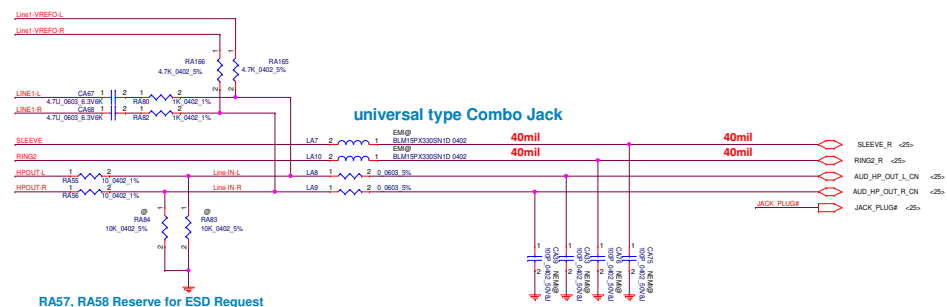


U49 Change SA00004BV00(NL17SZ07DFT2G_SC70-5) to from (NL17SZ07DFT2G_SC70-5)

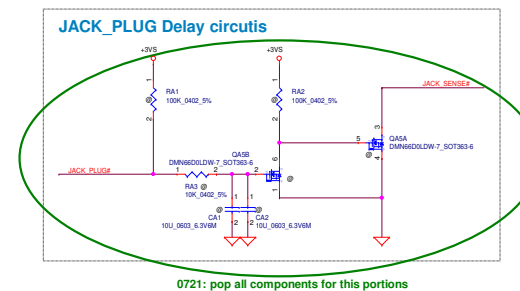
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2014/11/10	Deciphered Date	2015/11/25	Title	P22-eMMC
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Date: Tuesday, June 16, 2015					Sheet 22 of 44



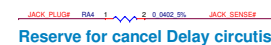
0724: change the cymbal to correct IC part and schematics



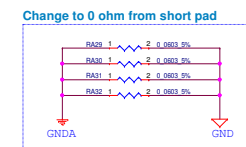
RA57, RA58 Reserve for ESD Request



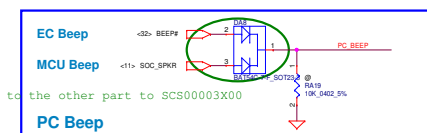
0721: pop all components for this portions



Reserve for cancel Delay circuitis

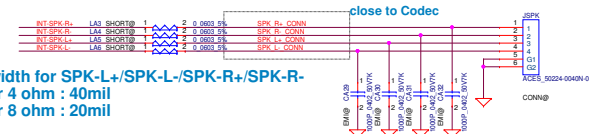


Place on the moat between GND & GNDA.

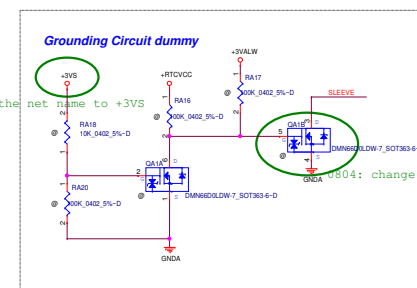


0718: change to the other part to SCS00003X00

Close to UA1
Pin11,13,14,16



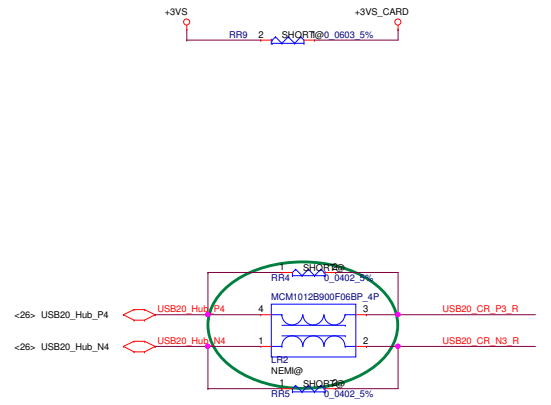
Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-
Speaker 4 ohm : 40mil
Speaker 8 ohm : 20mil



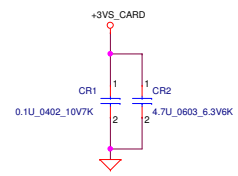
0718: change the net name to +3VS

Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2014/11/10	Deciphered Date	2015/11/25	P23-Audio Codec ALC3234	
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			Date:	Sheet	20 of 44

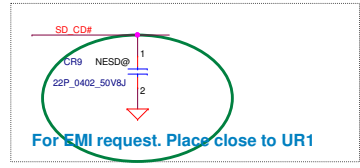
Main Func = Card Reader



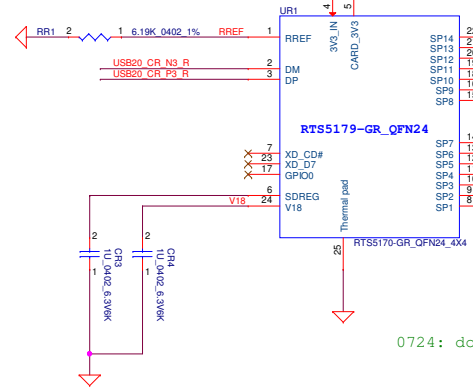
0725: change to the other part to SM070004800



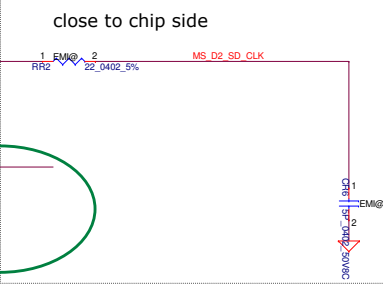
Trace width:40mil



For EMI request. Place close to UR1

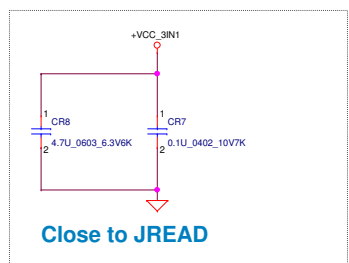


0724: vendor review to remove for compatibility

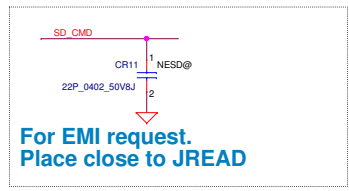


close to chip side

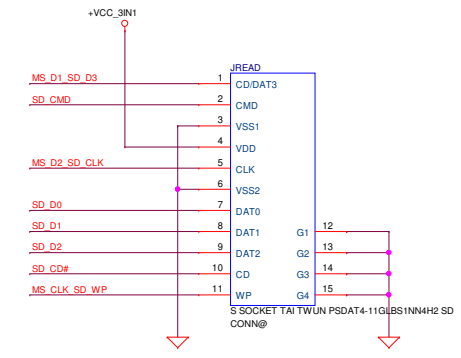
0724: doesn't support MS function and remove



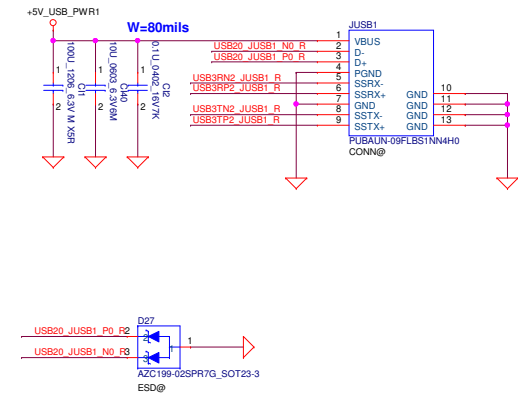
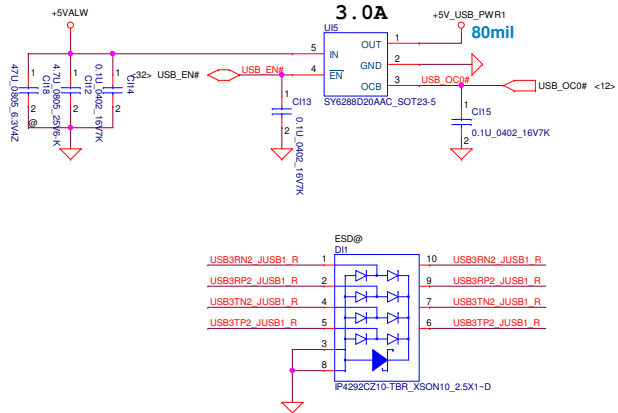
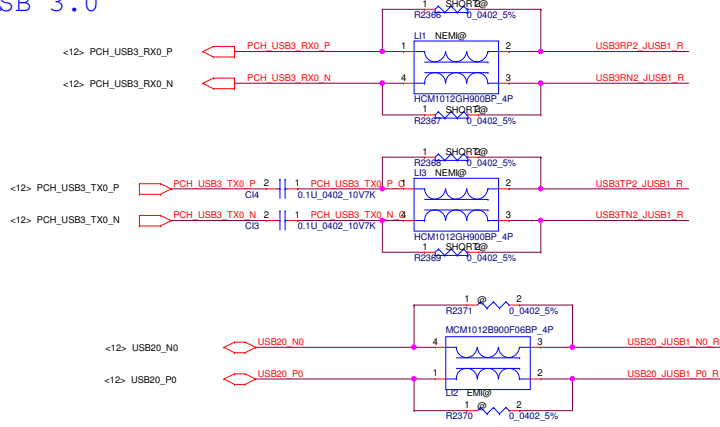
Close to JREAD



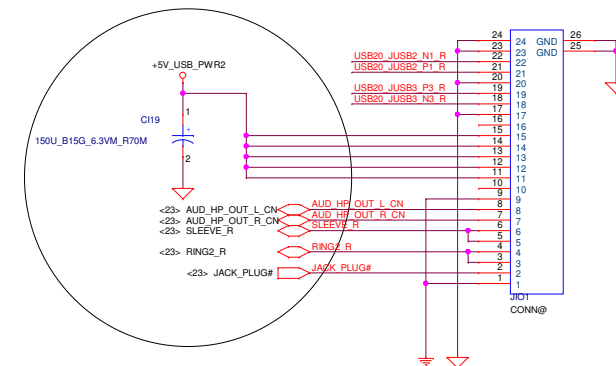
For EMI request. Place close to JREAD



USB 3.0

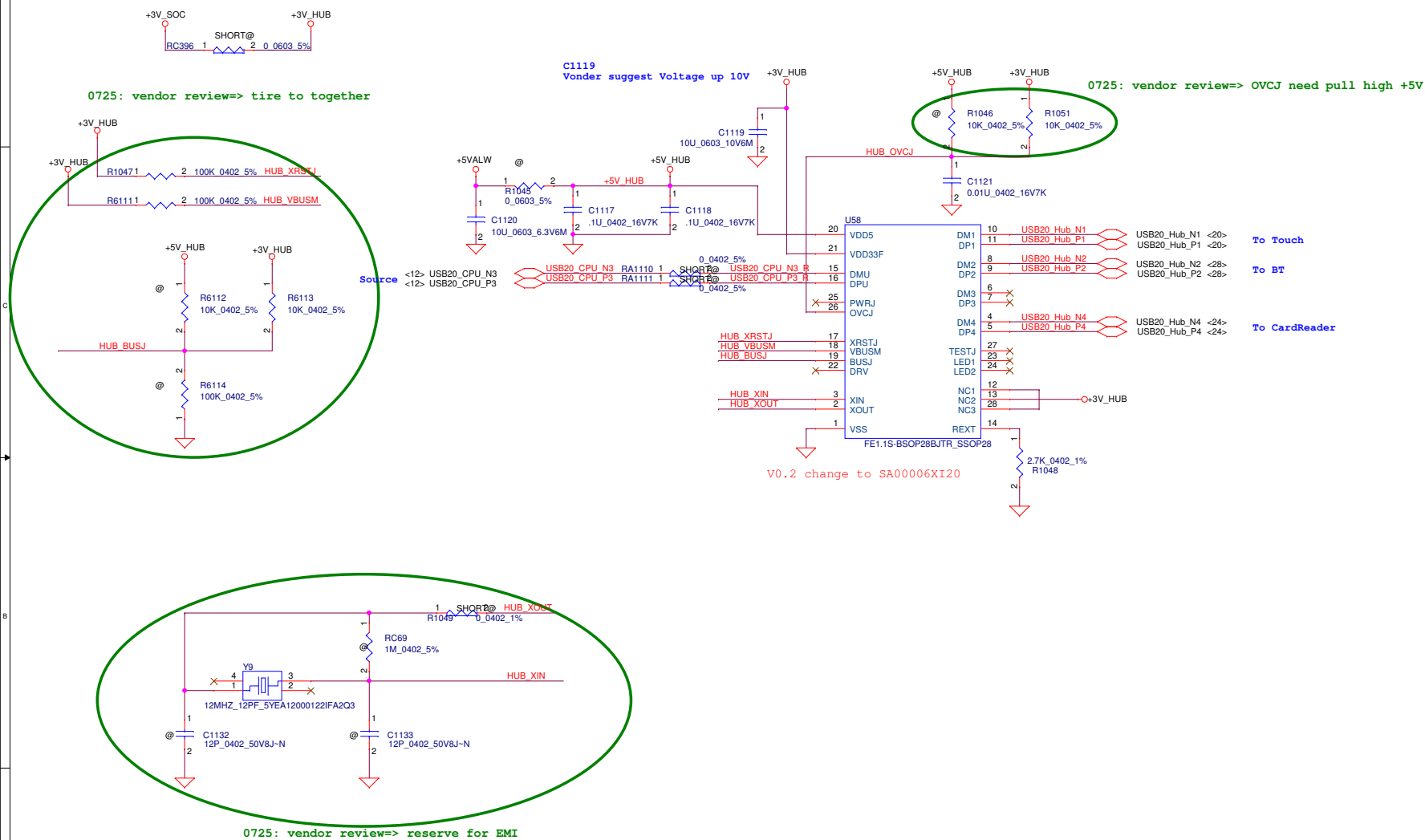


Pin 1 connection diagram for CVLVL_C18M12-VRA-NH. The diagram shows a 6-pin connector with pins 1 through 6. Pin 1 is labeled 'GND' and 'GND'. Pin 2 is labeled 'GND'. Pin 3 is labeled 'GND'. Pin 4 is labeled 'GND'. Pin 5 is labeled 'GND'. Pin 6 is labeled 'GND'. The connector is labeled 'JKDB1'. The board is labeled 'CVLVL_C18M12-VRA-NH' and 'CONN@'.

[illegible]

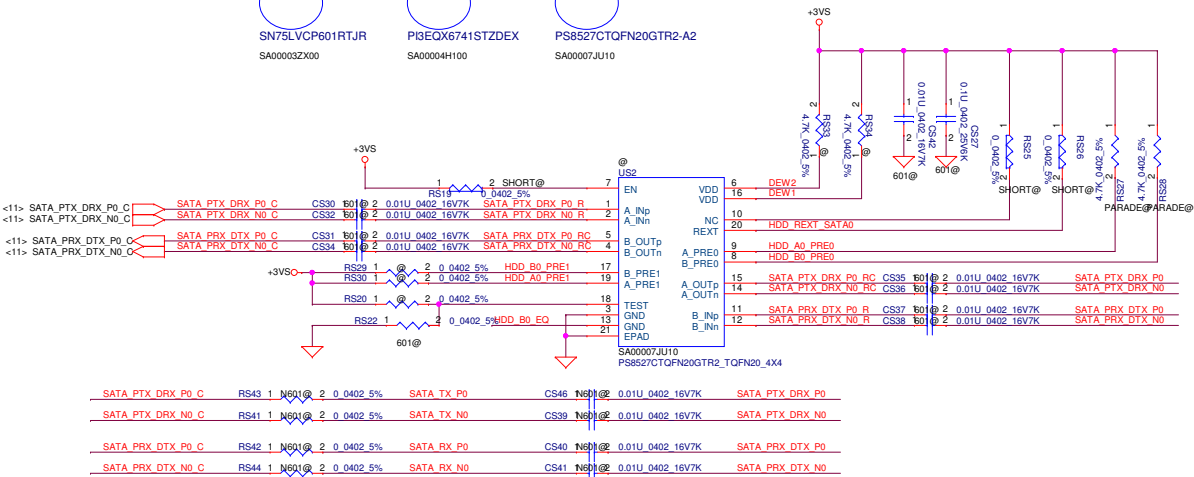
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				LA-C57IP	
				Date	Tuesday, June 16, 2015
				Sheet	26 of 44

Main Func = HUB 2.0



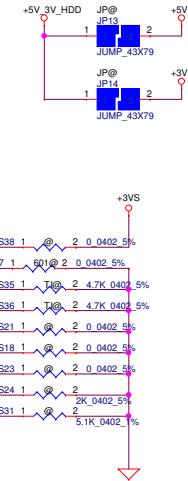
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2014/11/10	Deciphered Date	2015/11/25	Title	
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				LA-C571P	1.0
				Date: Tuesday, June 16, 2015	Sheet 26 of 44

Main Func = HDD

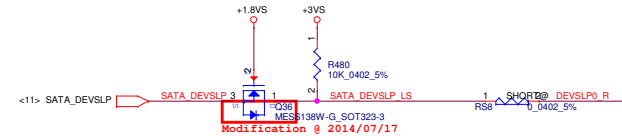
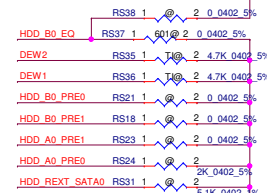
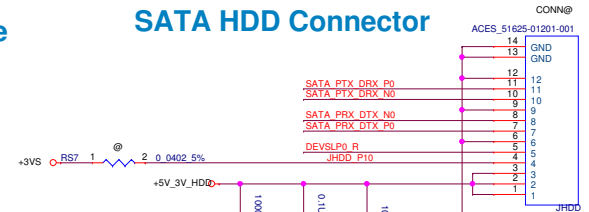


	DE	EQ
PARADE	-6dB	2.4dB
TI	-4dB	0dB

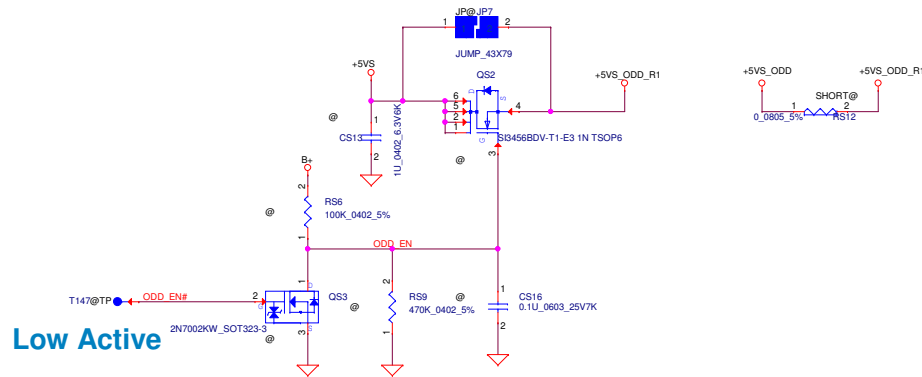
+5V_HDD Source



SATA HDD Connector

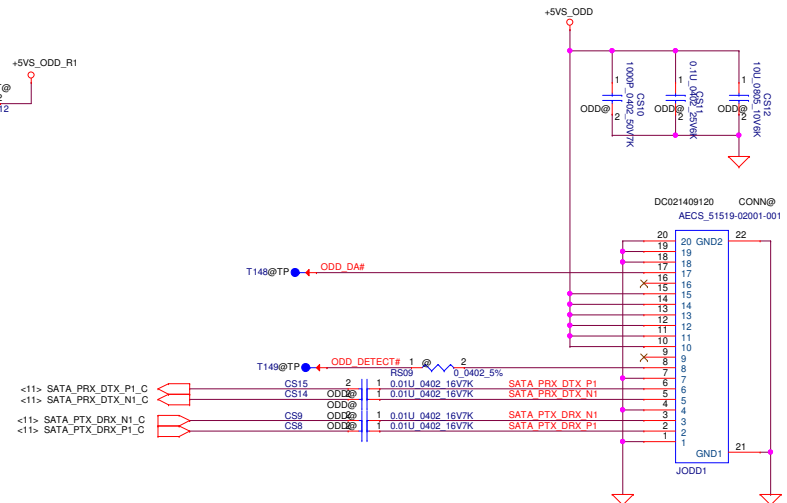


ODD Power Control



Low Active

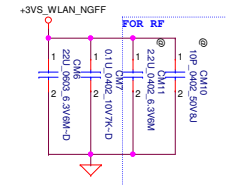
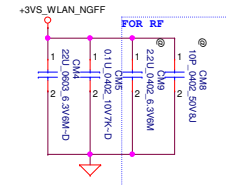
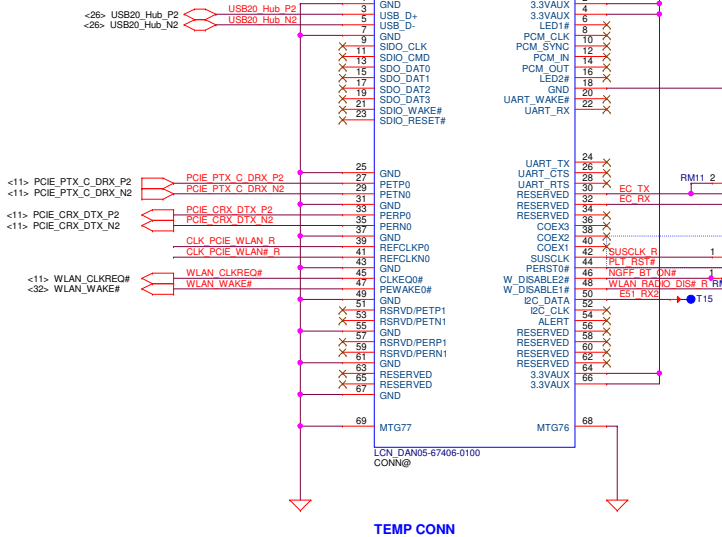
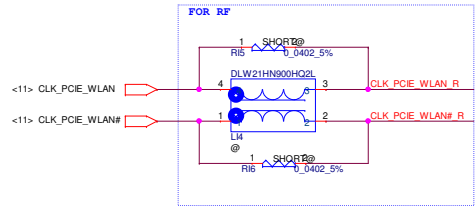
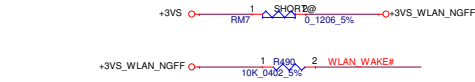
SATA ODD Connector



Main Func = NGFF

closed to pin 2, 4

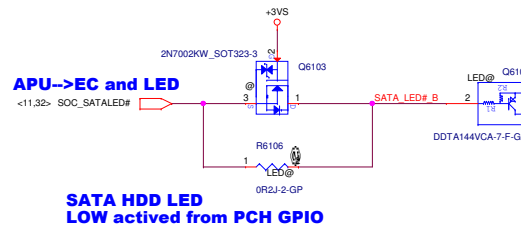
closed to pin 64, 66



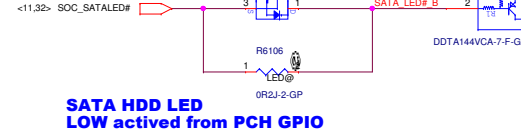
0721: change power rail to +3VS_WLAN_NGFF



HDD LED



APU-->EC and LED

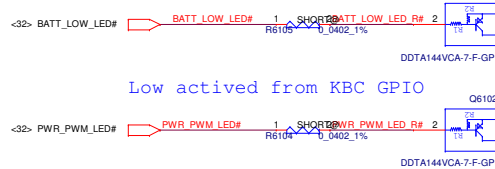


SATA HDD LED LOW activated from PCH GPIO

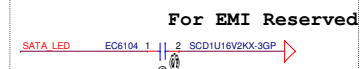
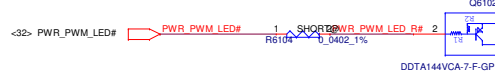
<11,32> SOC_SATALED#

Power / Battery LED

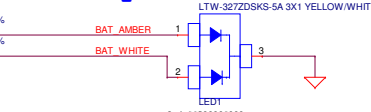
Low activated from KBC GPIO



Low activated from KBC GPIO



Battery LED1 (YELLOW LED)



Battery LED2 (WHITE_LED)

(WHITE_LED)



From EC



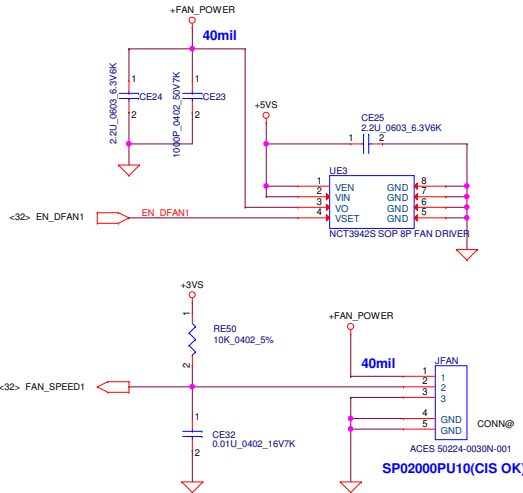
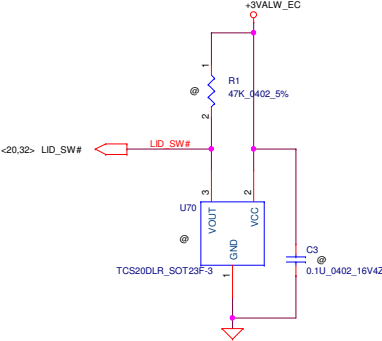
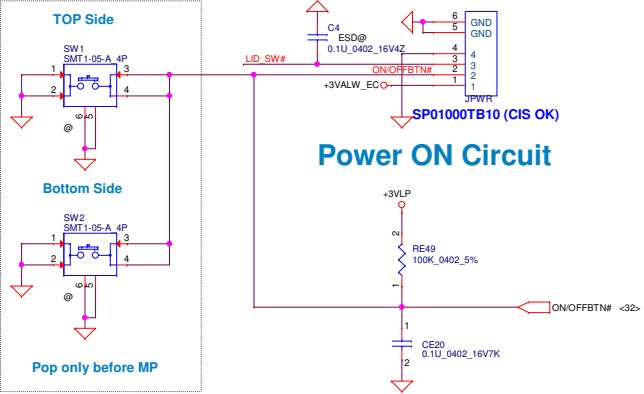
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				P28-Mini Card/LED
				LA-C571P
				Rev 1.0
				Date: Tuesday, June 16, 2015
				Sheet 28 of 44

Main Func = Touch Pad

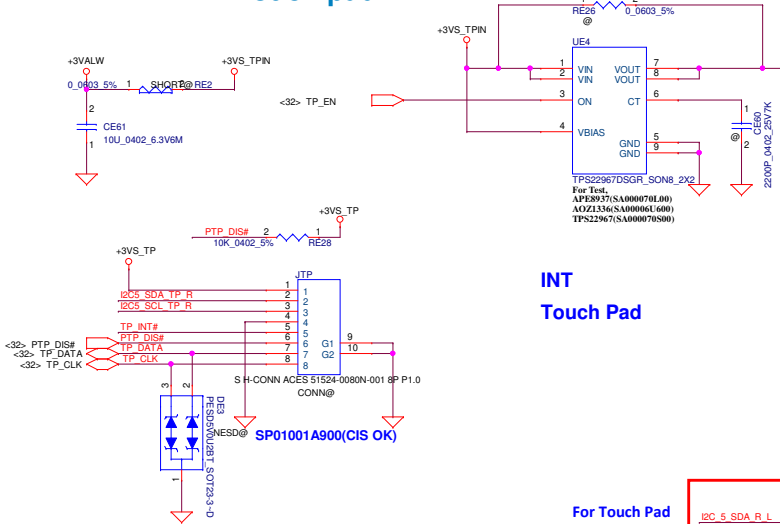
LID Switch

FAN Control circuit

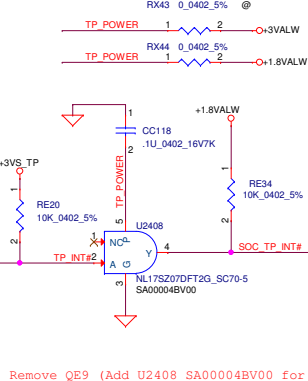
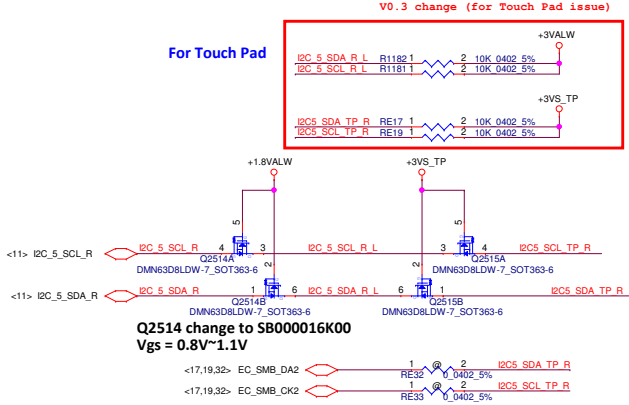
ON/OFF switch



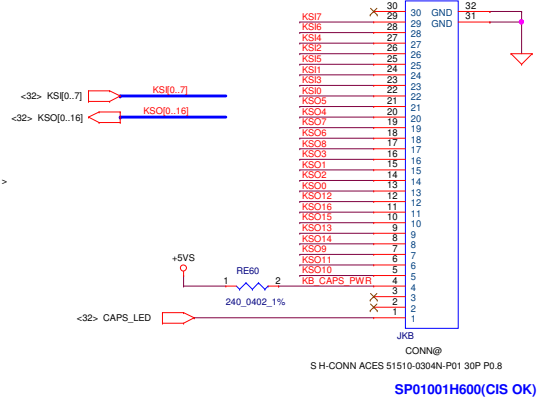
Touch pad



INT Touch Pad



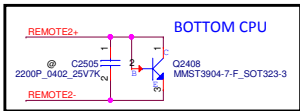
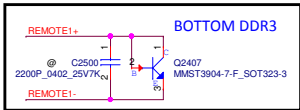
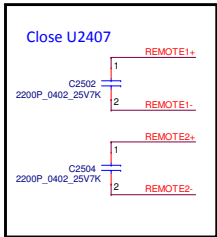
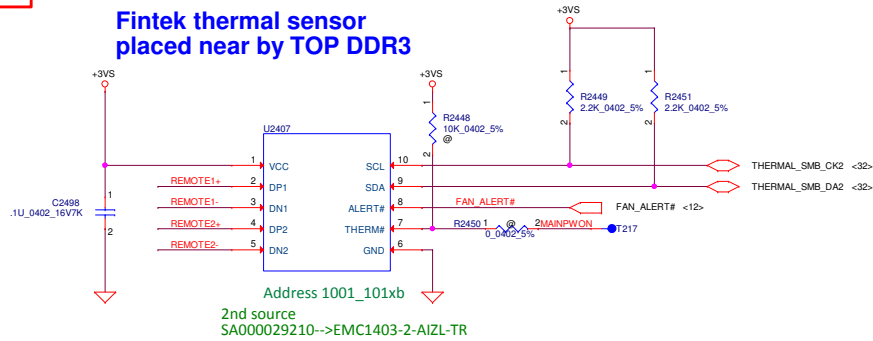
INT_KBD Connector



Event	PCH-TP_INT#	PCH-TP_INT#
S0	Interrupt	X
S3	X	Wake
1. Clamshell closed or Lid closed 2. Tablet mode for Convertible design 3. Disable TP function by ht-key	X	X

Main Func = Thermal

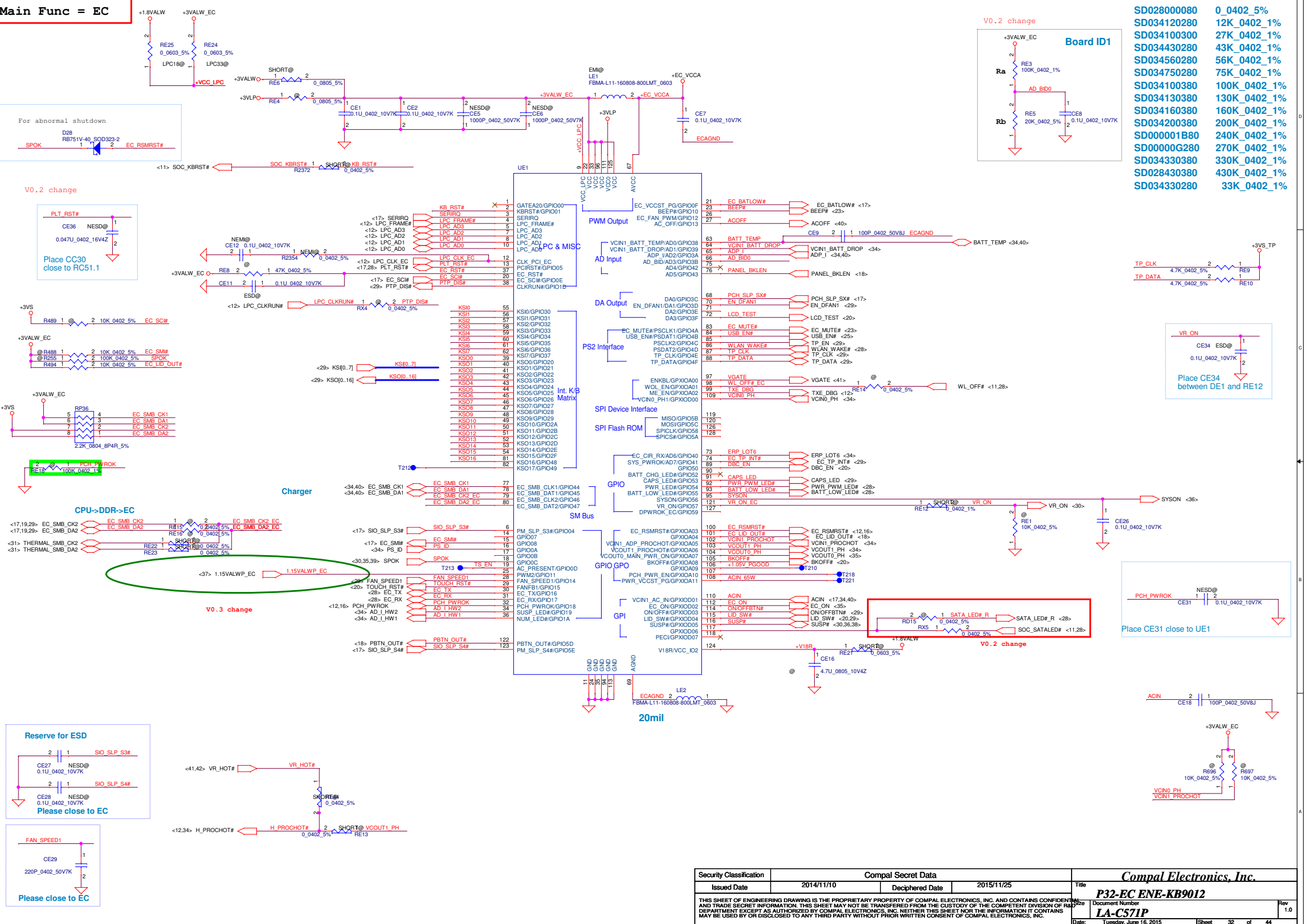
Fintek thermal sensor
placed near by TOP DDR3



REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"

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				LA-CS71P	1.0
Date: Tuesday, June 16, 2015				Sheet	31 of 44

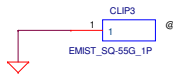
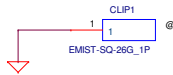
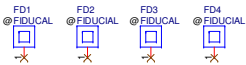
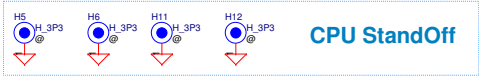
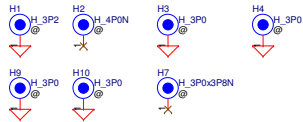
Main Func = EC



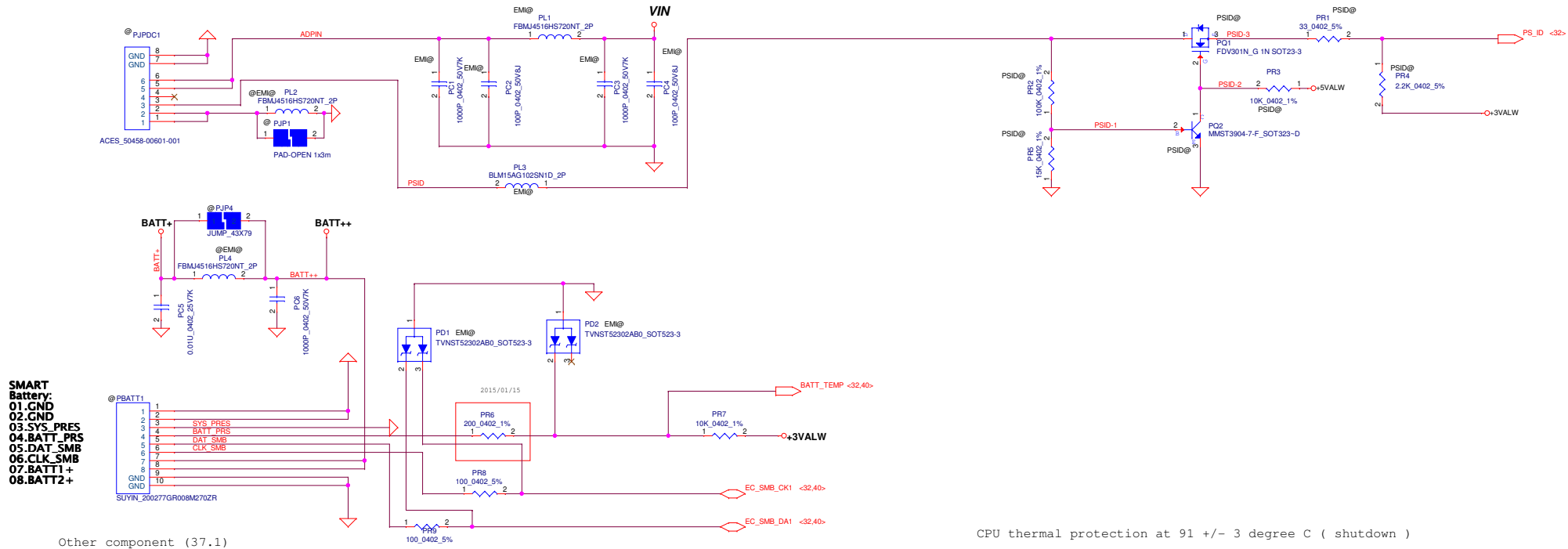
SD028000080	0_0402_5%
SD03410280	12K_0402_1%
SD034100300	27K_0402_1%
SD034403080	43K_0402_1%
SD034560280	56K_0402_1%
SD034750280	75K_0402_1%
SD034100380	100K_0402_1%
SD034130380	130K_0402_1%
SD034160380	160K_0402_1%
SD034200380	200K_0402_1%
SD000001B80	240K_0402_1%
SD00000G280	270K_0402_1%
SD034330380	330K_0402_1%
SD028430380	430K_0402_1%
SD034330280	33K_0402_1%

Main Func = Screw Hole

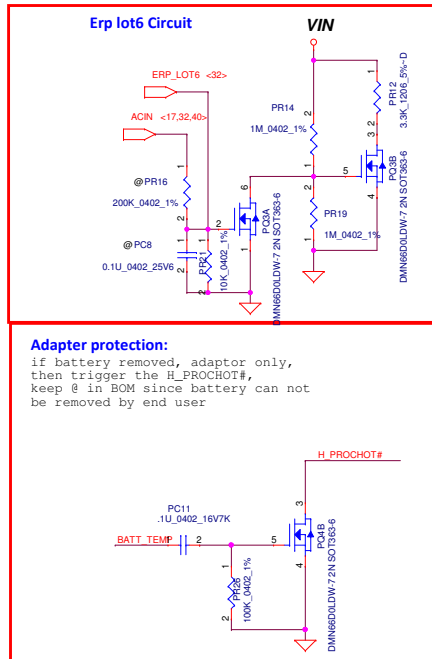
Screw Hole



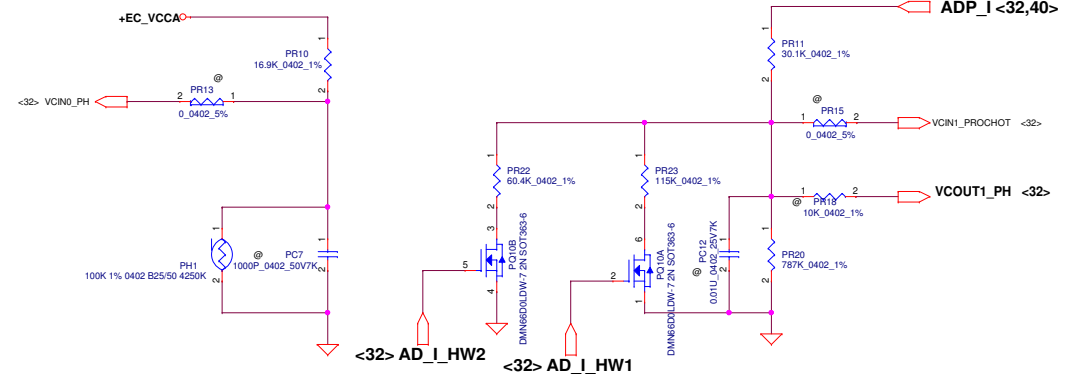
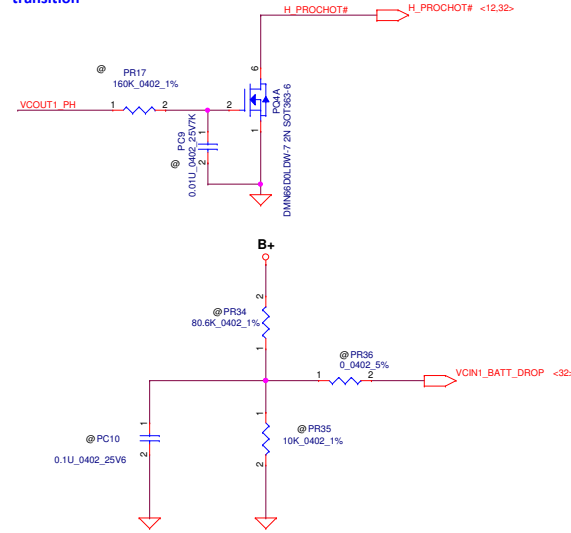
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Issued Date		2014/11/10	Deciphered Date	2015/11/25	Rev
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CPU thermal protection at 91 +/- 3 degree C (shutdown)



Delay adaptor OC H_PROCHOT#
 2ms while hybrid power
 transition



ADP_I(with selector) to support "PWC" function.

H_PROCHOT#	AD_I_HW1	AD_I_HW2
35W	0	0
45W	1	0
55W	0	1
65W	1	1

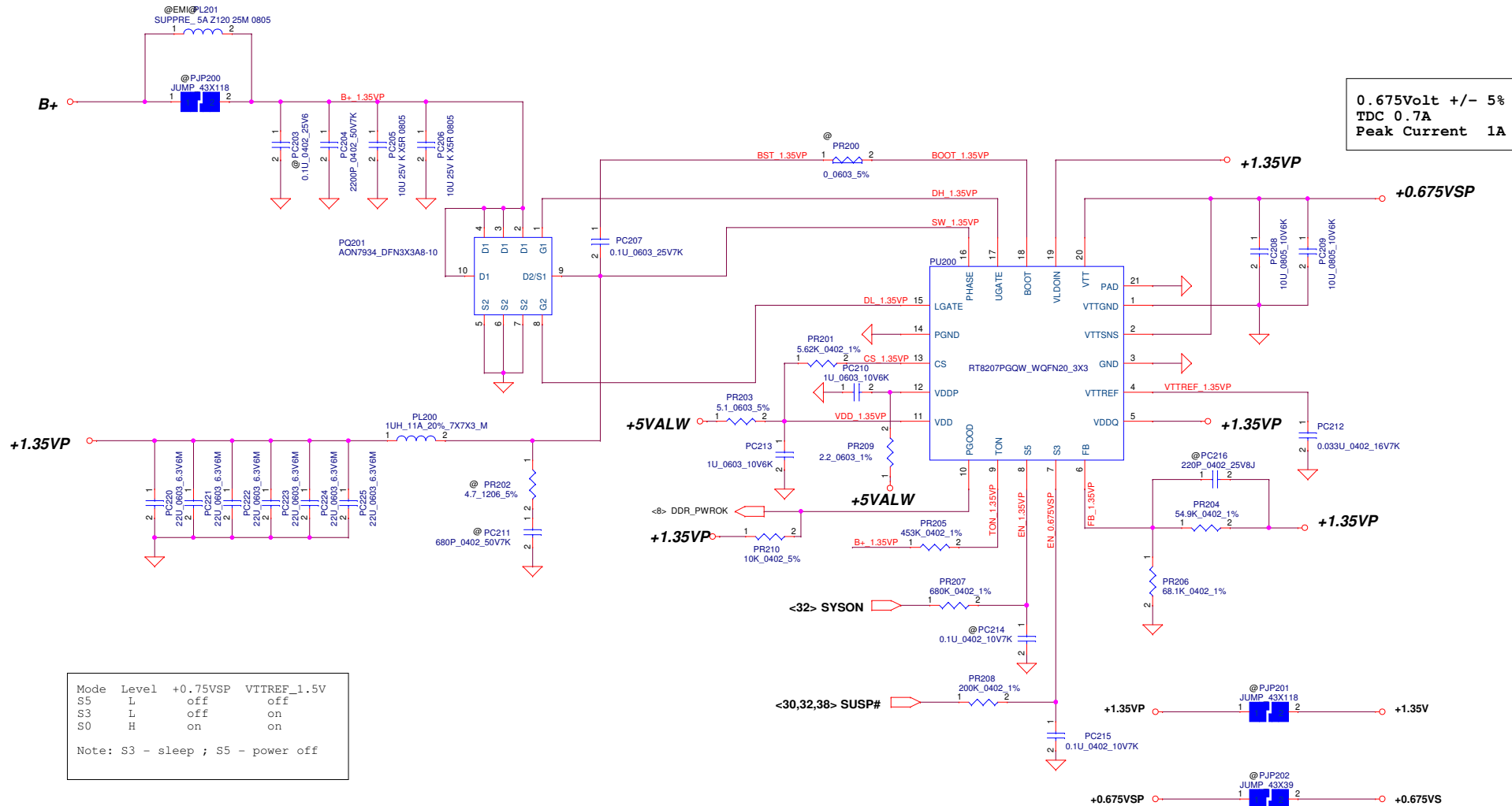
DELL CONFIDENTIAL/PROPRIETARY

```
5VALWP
TDC 5.3A
Peak Current 6.62A
OCP current 8.61A
```



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1.35VP
TDC 3.6A
Peak Current 4.5A
OCP current 6A

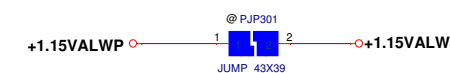
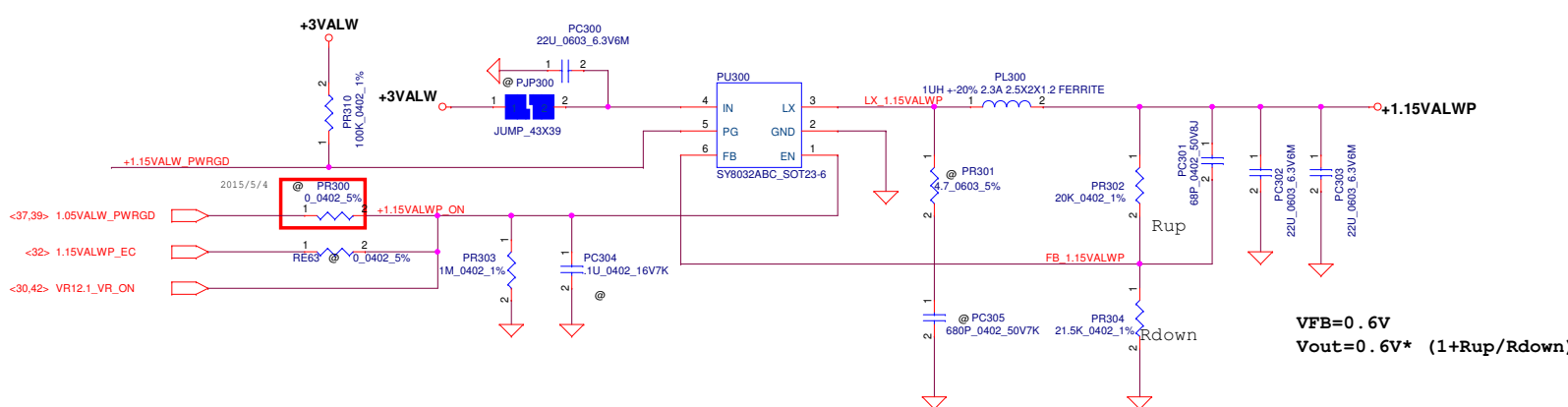


Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

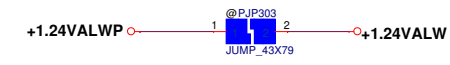
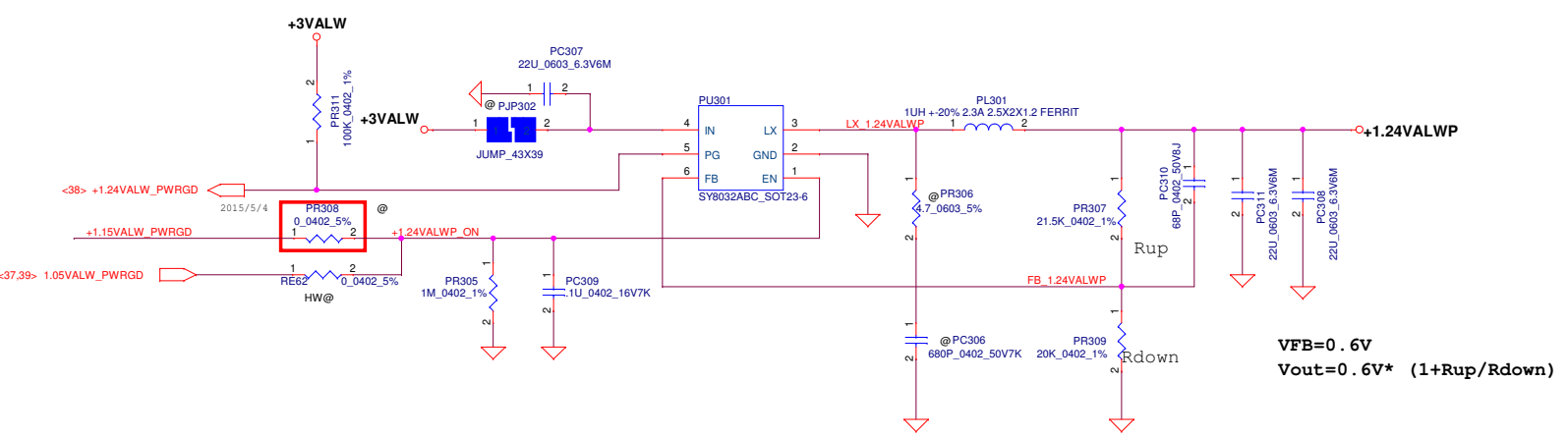
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					Size	Document Number	Rev	
					Custom	LA-B911P	1.0	
Date:		Sheet	36	of	44			



+1.15VALWP
 TDC 0.64A
 Peak Current 0.8A
 OCP current 3.5A

$V_{FB}=0.6V$
 $V_{out}=0.6V * (1+R_{up}/R_{down})$

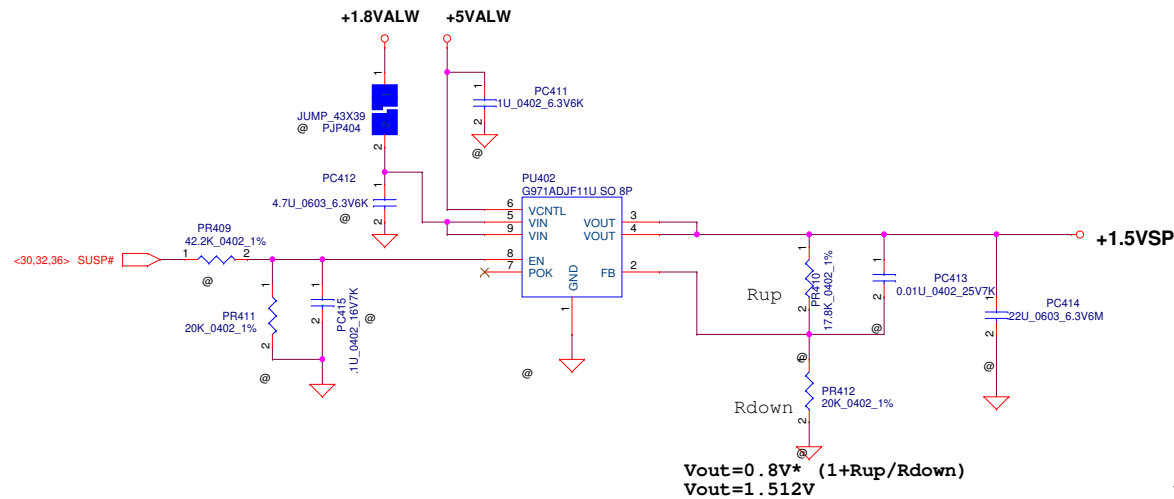
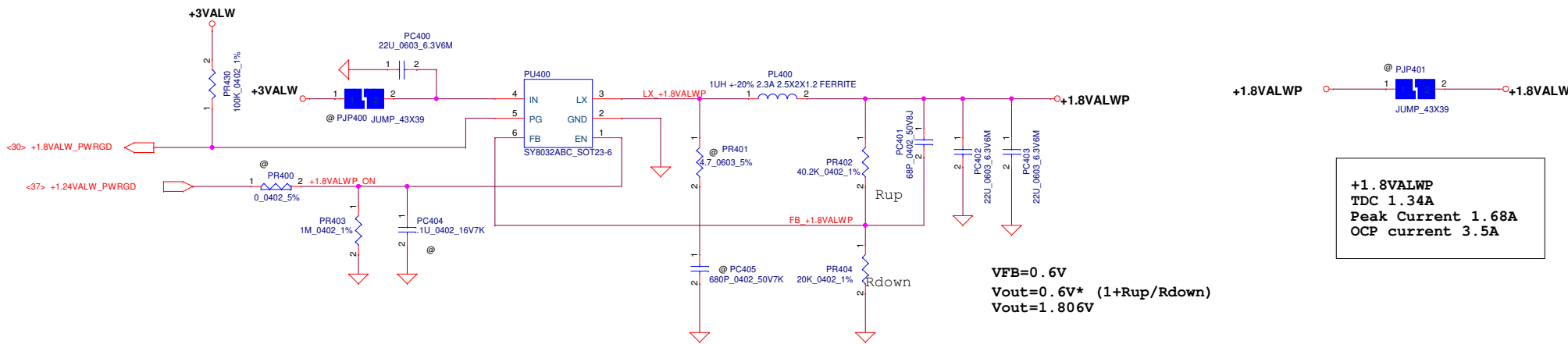


+1.24VALWP
 TDC 0.72A
 Peak Current 0.9A
 OCP current 3.5A

$V_{FB}=0.6V$
 $V_{out}=0.6V * (1+R_{up}/R_{down})$

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				Document Number
				Custom
				Rev
				1.0
				Date:
				Sheet 37 of 44

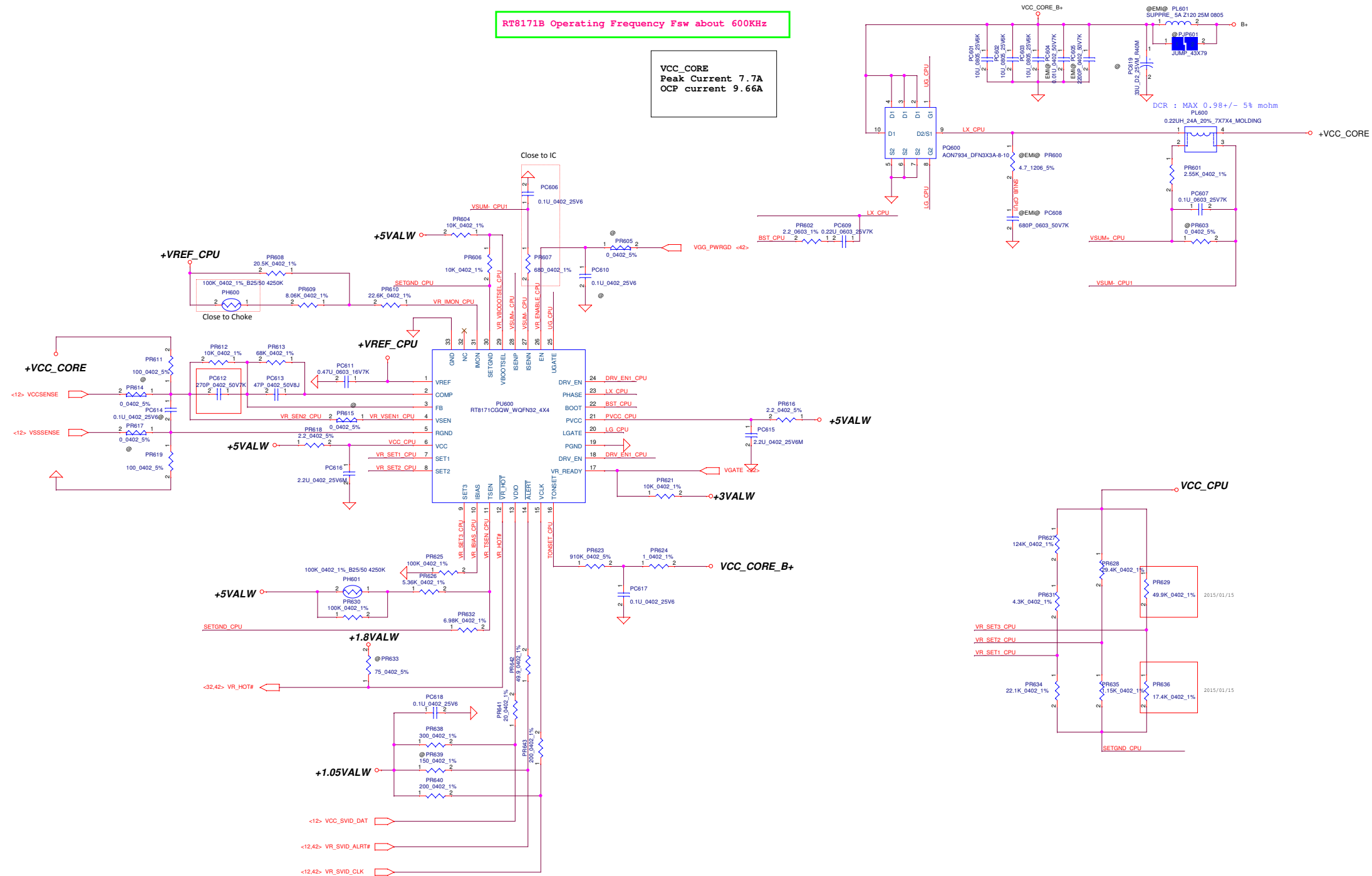


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								P38-PWR-1.8VALW/1.5VSP			
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						Custom		LA-B911P			
						Date:		Tuesday, June 16, 2015		Sheet 38 of 44	

RT8171B Operating Frequency Fsw about 600KHz

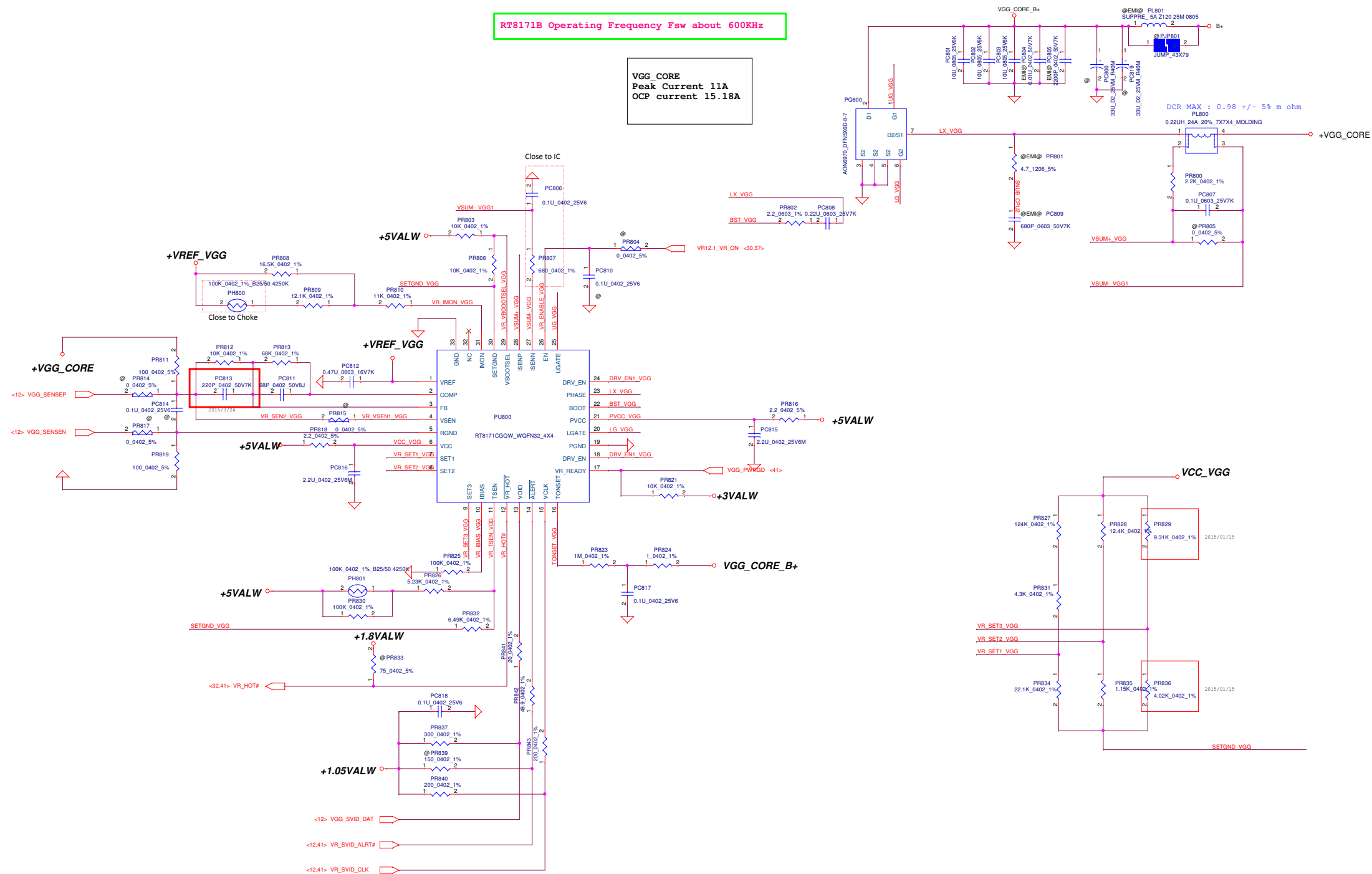
VCC_CORE
Peak Current 7.7A
OCP current 9.66A



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Issued Date		2011/07/08		Deciphered Date		2015/07/08		Title					
								CPU COREP					
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								Custom		LA-C571P		0.1	
				Date:		Tuesday, June 16, 2015		Sheet		41 of 44			

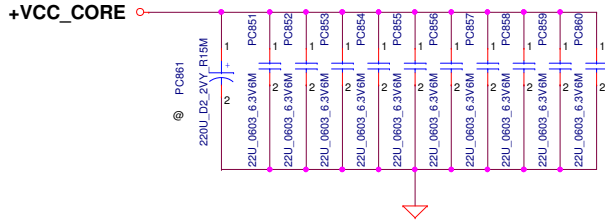
RT8171B Operating Frequency Fsw about 600KHz

```
VGG_CORE
Peak Current 11A
OCP current 15.18A
```

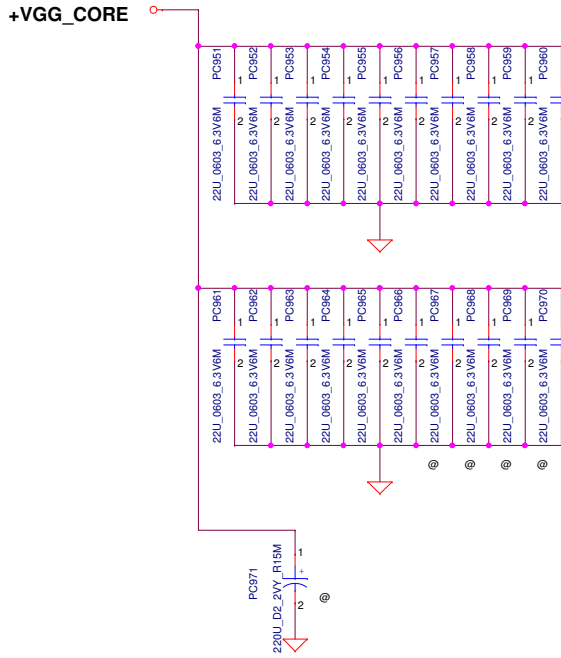


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				Date: Tuesday, June 16, 2015	Sheet 42 of 44

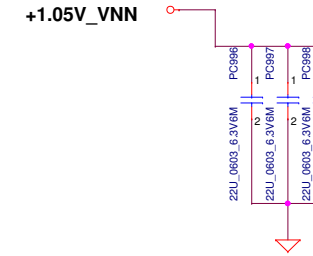
22U_0603 * 14 + reserved+220uF 15m ohm



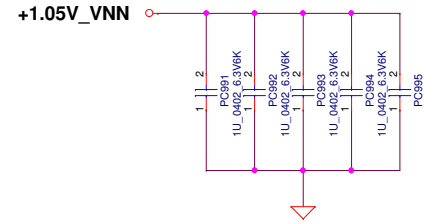
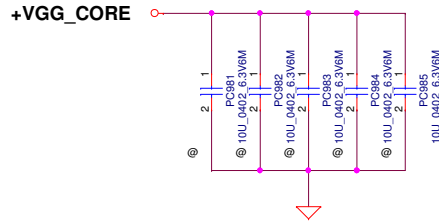
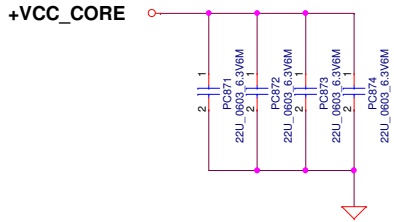
22U_0603 * 16 +4 reserved+220uF 15m ohm



22U_0603 * 3



Place on CPU Back Side.



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/08	Deciphered Date	2015/07/08	Title	PWR-PROCESSOR DECOUPLING
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		For PS2/PS3 ripple			PR829 change 976 from to 9.31Kohm , PR836 change 412 from to 4.02K ohm	15/01/15	EVT
2		For PS2/PS3 ripple			PR629 change 39.2k from to 48.9Kohm , PR636 change 14k from to 17.4K ohm , PC612 change form 470pF to 270pF	15/01/15	EVT
3		Compal ESD team request			PR6 change 100ohm from to 200 ohm	15/01/15	EVT
4		For HW power sequency			PR300 change to reserve	4/05/15	DVT2
5		For HW power sequency			PR308 change to reserve	4/05/15	DVT2
5							
6							
7							